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Cadence Design Systems

GPDK 90 nm Mixed Signal GPDK Spec

DRC Revision History

Revision History

RELEASE NOTES FOR THE 90nm GPDK

VERSION v4.4

- gpdk090 OA22 library built natively with IC6.1.3.500.1 release code
- gpdk090 CDB library built natively with IC5.10.41_USR5.90.69 release code
- Removed extraneous subckt parameters from mimcap spectre model
- Removed extraneous subckt parameters from diode spectre model
- Updated Circuit prospector entries in libInitCustomExit.il (CCR 605869)
- Updated ijth settings in MOS models to remove extraneous warnings
- Updated Assura compare rules for CDL netlister (CCR 607542)
- Added must connect group for pcell body tie pins (CCR 609600)
- Resistor contact resistance set to zero to avoid double counting in RCX

VERSION v4.3

- gpdk090 OA22 library built natively with IC6.1.2.500.17 release code
- gpdk090 CDB library built natively with IC5.10.41_USR5.90.69 release code
- Renamed LEFDefaultRouteSpec to LEFDefaultRouteSpec_gpdk090 (CCR 594263)
- Spectre models updated for corners, MC, mismatch, and noise
- Techfile updates made in preparation for IC6.1.3 release
- Removed CDF extraneous simulation MOS parameters (CCR 595042)
- Created new QRC database with 3d field solver information (CCR 582163)
- Added missing 2 terminal resistor pcell schematics (CCR 537806)

VERSION v4.2

- gpdk090 OA22 library built natively with IC6.1.2.500.9 release code
- gpdk090 CDB library built natively with IC5.10.41_USR5.90.69 release code
- Added transistorDSPF option for the extraction in the GPDK090 (CCR 551957)
- Changed Assura compare.rul file to fix parallel cap combine error (CCR 553798)
- Updated Poly to Oxide spacing for DFM to fix inadvertent change (CCR 555400)

VERSION v4.1

- gpdk090 OA22 library built natively with IC6.1.2.500.8 release code
- gpdk090 CDB library built natively with IC5.10.41_USR5.90.69 release code
- Added several MOS and Res devices with Inherted Connections (CCR 537806)
- Renamed the ASCII techfiles to support the DFII GUI file lookup (CCR 542850)
- Added CDF AreaFormula parameter to support ADE-GXL optimization (CCR 468274)
- Added Metal Layer CurrentDensity information to the IC61 techfile
- Fixed issue with multi-abutment of MOS devices (CCR 530084)
- The following model updates made: (CCR 549179)
    1. Resistor corners fixed and corner names changed to "h" and "l"
        Note: h=high, l=low (old values are "b" and "w").
    2. MIMCAP corners added
    3. MOS gate leakage added/fixed
    4. MOS 1/f noise added...

Generator Info

Generator Information

Sample runset for 90 nm technology Default Grid: 0.005 Valid Angle: 45 Flag Acute: true Flag Self-intersecting: true

Global Parameters

Global Parameters

libName	gpdk090	Primitive Library Name	

Introduction

This document defines the Design Rules and Electrical Parameters for a generic, foundary independent 90nm CMOS Mixed-Signal process.

This document is divided into three sections:

* CMOS Digital Core Design Rules

  describes the widths, spacings, enclosures, overlaps, etc. needed to create the physical layout of the core section of a digital CMOS design.

* CMOS I/O Design Rules

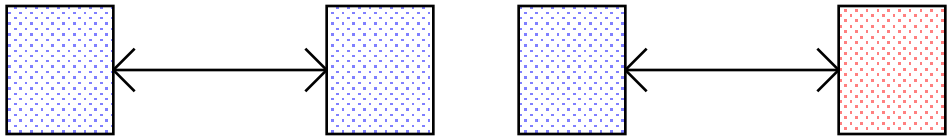
  describes the widths, spacings, enclosures, overlaps, etc. needed to create the physical layout of the I/O section of a CMOS design.

* CMOS Digital Electrical Parameters

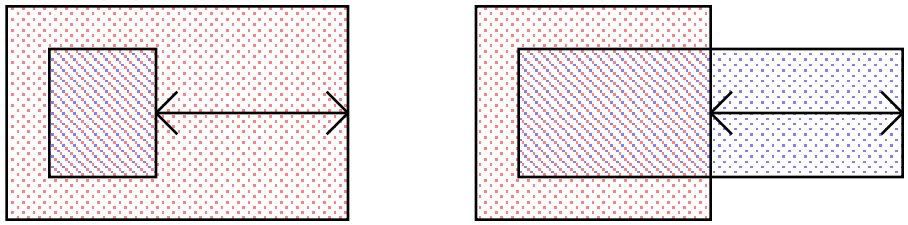
  describes the electrical parameters of a digital CMOS design.

Terminology Definitions

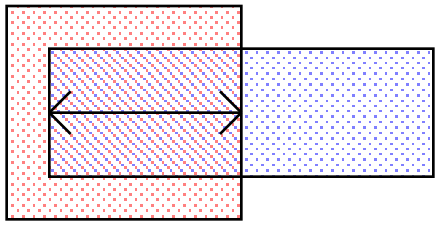
Spacing - distance from the outside of the edge of a shape to the outside of the edge of another shape.



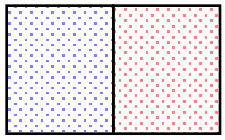
Enclosure - distance from the inside of the edge of a shape to the outside of the edge of another shape.



Overlap - distance from the inside of the edge of a shape to the inside of the edge of another shape.



Butting - outside of the edge of a shape touching the outside of the edge of another shape.



Layer Descriptions

This table describes the layers used to create devices.

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
Bondpad	36	0	Bondpad	Bondpad	drawing	95	252	Bonding Pad
CapMetal	14	0	CapMetal	CapMetal	drawing	97	252	MiM capacitor metal
Nburied	19	0	Nburied	Nburied	drawing	18	252	N+ Buried Layer
Nhvt	18	0	Nhvt	Nhvt	drawing	11	252	NMOS High Vt
Nimp	4	0	Nimp	Nimp	drawing	12	252	N+ Implant
Nwell	2	0	Nwell	Nwell	drawing	6	252	Nwell
Nzvt	52	0	Nzvt	Nzvt	drawing	15	252	NMOS Zero Vt
Oxide	1	0	Oxide	Oxide	drawing	2	252	Active Area
Oxide_thk	24	0	Oxide_thk	Oxide_thk	drawing	4	252	2.5V Active Area
Phvt	23	0	Phvt	Phvt	drawing	13	252	PMOS High Vt
Pimp	5	0	Pimp	Pimp	drawing	14	252	P+ Implant
Poly	3	0	Poly	Poly	drawing	10	252	Poly
SiProt	72	0	SiProt	SiProt	drawing	16	252	Salicide Block

Table 1: Device Layers

This table describes the layers used to interconnect devices.

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
Cont	6	0	Cont	Cont	drawing	20	252	Metal Contact to Oxide/Poly
Metal1	7	0	Metal1	Metal1	drawing	30	252	1st Metal for interconnect
Metal1_slot	7	2	M1_slot	Metal1	slot	30	1	1st Metal stress relief
Metal2	9	0	Metal2	Metal2	drawing	34	252	2nd Metal for interconnect
Metal2_slot	9	2	M2_slot	Metal2	slot	34	1	2nd Metal stress relief
Metal3	11	0	Metal3	Metal3	drawing	38	252	3rd Metal for interconnect
Metal3_slot	11	2	M3_slot	Metal3	slot	38	1	3rd Metal stress relief
Metal4	31	0	Metal4	Metal4	drawing	42	252	4th Metal for interconnect
Metal4_slot	31	2	M4_slot	Metal4	slot	42	1	4th Metal stress relief
Metal5	33	0	Metal5	Metal5	drawing	46	252	5th Metal for interconnect
Metal5_slot	33	2	M5_slot	Metal5	slot	46	1	5th Metal stress relief
Metal6	35	0	Metal6	Metal6	drawing	50	252	6th Metal for interconnect
Metal6_slot	35	2	M6_slot	Metal6	slot	50	1	6th Metal stress relief
Metal7	38	0	Metal7	Metal7	drawing	54	252	7th Metal for interconnect
Metal7_slot	38	2	M7_slot	Metal7	slot	54	1	7th Metal stress relief
Metal8	40	0	Metal8	Metal8	drawing	58	252	8th Metal for interconnect
Metal8_slot	40	2	M8_slot	Metal8	slot	58	1	8th Metal stress relief
Metal9	42	0	Metal9	Metal9	drawing	62	252	9th Metal for interconnect
Metal9_slot	42	2	M9_slot	Metal9	slot	62	1	9th Metal stress relief
Via1	8	0	Via1	Via1	drawing	32	252	Via between 1st and 2nd Metal
Via2	10	0	Via2	Via2	drawing	36	252	Via between 2nd and 3rd Metal
Via3	30	0	Via3	Via3	drawing	38	252	Via between 3rd and 4th Metal
Via4	32	0	Via4	Via4	drawing	44	252	Via between 4th and 5th Metal
Via5	34	0	Via5	Via5	drawing	48	252	Via between 5th and 6th Metal
Via6	37	0	Via6	Via6	drawing	52	252	Via between 6th and 7th Metal
Via7	39	0	Via7	Via7	drawing	54	252	Via between 7th and 8th Metal
Via8	41	0	Via8	Via8	drawing	60	252	Via between 8th and 9th Metal

Table 2: Interconnect Layers

This table describes the layers used to mark/label shapes for DRC and/or LVS..

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
BJTdum	15	0	BJTdum	BJTdum	drawing	92	252	Marks BJT emitters
VPNP2dum	60	0	VPNP2dum	VPNP2dum	drawing	108	252	Marks BJT vpnp2
VPNP5dum	61	0	VPNP5dum	VPNP5dum	drawing	109	252	Marks BJT vpnp5
VPNP10dum	62	0	VPNP10dum	VPNP10dum	drawing	110	252	Marks BJT vpnp10
Capdum	12	0	Capdum	Capdum	drawing	96	252	Marks capacitors
Cap3dum	84	0	Cap3dum	Cap3dum	drawing	93	252	Marks capacitors 3 term
DIOdummy	22	0	DIOdum	DIOdummy	drawing	82	252	Marks diodes
INDdummy	16	0	INDdum	INDdummy	drawing	90	252	Marks inductor terminal
IND2dummy	17	0	IND2dum	IND2dummy	drawing	88	252	Marks inductor terminal
IND3dummy	70	0	IND3dum	IND3dummy	drawing	114	252	Marks inductor terminal
ESDdummy	74	0	ESDdum	ESDdummy	drawing	115	252	Marks ESD and I/O devices
Metal1_text	7	3	Metal1	Metal1	drawing	30	252	Labels Metal1 nodes
Metal2_text	9	3	Metal2	Metal2	drawing	34	252	Labels Metal2 nodes
Metal3_text	11	3	Metal3	Metal3	drawing	38	252	Labels Metal3 nodes
Metal4_text	31	3	Metal4	Metal4	drawing	42	252	Labels Metal4 nodes
Metal5_text	33	3	Metal5	Metal5	drawing	46	252	Labels Metal5 nodes
Metal6_text	35	3	Metal6	Metal6	drawing	50	252	Labels Metal6 nodes
Metal7_text	38	3	Metal7	Metal7	drawing	54	252	Labels Metal7 nodes
Metal8_text	40	3	Metal8	Metal8	drawing	58	252	Labels Metal8 nodes
Metal9_text	42	3	Metal9	Metal9	drawing	62	252	Labels Metal9 nodes
NPNdummy	20	0	NPNdum	NPNdummy	drawing	86	252	Marks NPN devices
PNPdummy	21	0	PNPdum	PNPdummy	drawing	84	252	Marks PNP devices
Psub	25	0	Psub	Psub	drawing	80	252	Marks seperate substrate areas
Resdum	13	0	Resdum	Resdum	drawing	94	252	Marks Poly/Oxide resistor area
ResWdum	71	0	ResWdum	ResWdum	drawing	98	252	Marks Nwell resistor area
text	63	0	text	text	drawing	230	252	Text for information

Table 3: DRC/LVS Marker/Label Layers

Device Layer Table

This table describes the layers used in each device.

0: the layer must not touch the device structure
1: the layer must enclose or straddle the device structure
-: the layer may either enclose or avoid the device structure

	NMOS (1.2V)	PMOS (1.2V)	LP NMOS (1.2V)	LP PMOS (1.2V)	NMOS (2.5V)	PMOS (2.5V)	Native NMOS (1.2V)	Native NMOS (2.5V)
Nburied	0	0	0	0	0	0	0	0
Nwell	0	1	0	1	0	1	0	0
Oxide	1	1	1	1	1	1	1	1
Oxide_thk	0	0	0	0	1	1	0	1
Poly	1	1	1	1	1	1	1	1
Nimp	1	0	1	0	1	0	1	1
Pimp	0	1	0	1	0	1	0	0
Nzvt	0	0	0	0	0	0	1	1
Nhvt	0	0	1	0	0	0	0	0
Phvt	0	0	0	1	0	0	0	0
SiProt	0	0	0	0	0	0	0	0

Table 4: MOS Device Layers

	N+/PW Diode	P+/NW Diode
Nburied	0	0
Nwell	0	1
Oxide	1	1
Oxide_thk	0	0
Poly	0	0
Nimp	1	0
Pimp	0	1
Nzvt	0	0
Nhvt	0	0
Phvt	0	0
SiProt	0	0

Table 5: Diode Device Layers

	Salicided N+ Poly Resistor	Salicided P+ Poly Resistor	Salicided N+ Oxide Resistor	Salicided P+ Oxide Resistor	Non-Salicided N+ Poly Resistor	Non-Salicided P+ Poly Resistor	Non-Salicided N+ Oxide Resistor	Non-Salicided P+ Oxide Resistor
Nburied	0	0	0	0	0	0	0	0
Nwell	-	-	0	1	-	-	0	1
Oxide	0	0	1	1	0	0	1	1
Oxide_thk	0	0	0	0	0	0	0	0
Poly	1	1	0	0	1	1	0	0
Nimp	1	0	1	0	1	0	1	0
Pimp	0	1	0	1	0	1	0	1
Nzvt	0	0	0	0	0	0	0	0
Nhvt	0	0	0	0	0	0	0	0
Phvt	0	0	0	0	0	0	0	0
SiProt	0	0	0	0	1	1	1	1

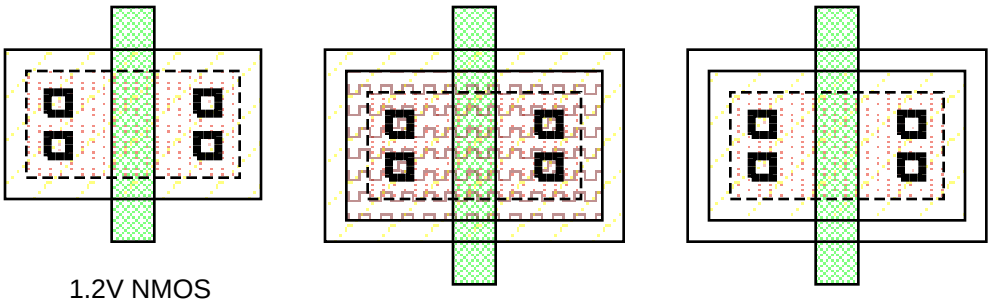
	Nwell in Oxide Resistor	Nwell in STI Resistor
Nburied	0	0
Nwell	1	1
Oxide	1	1
Oxide_thk	0	0
Poly	0	0
Nimp	1	1
Pimp	0	0
Nzvt	0	0
Nhvt	0	0
Phvt	0	0
SiProt	1	0

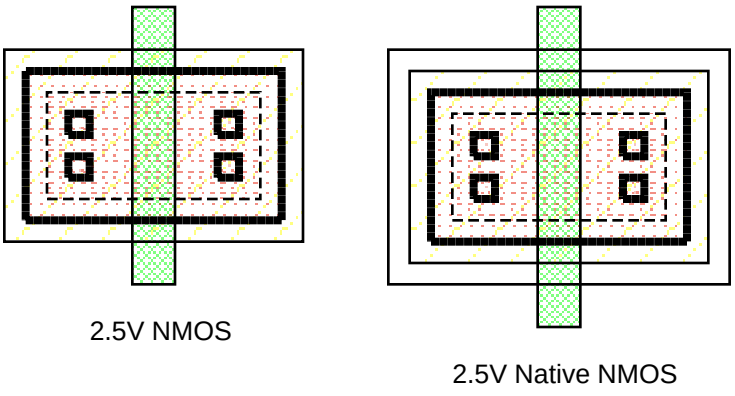
Table 6: Resistor Device Layers

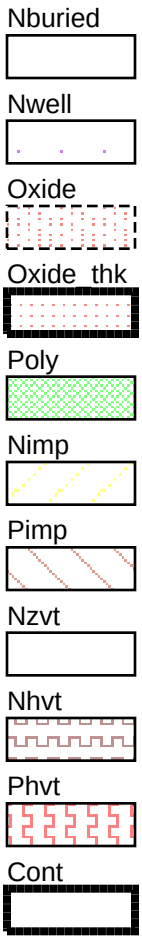
	SPNP	VNPN	Varactor (NMOSCAP)
Nburied	0	1	0
Nwell	1	1	1
Oxide	1	1	1
Oxide_thk	0	0	0
Poly	0	0	1
Nimp	1	1	1
Pimp	1	1	0
Nzvt	0	0	0
Nhvt	0	0	0
Phvt	0	0	0
SiProt	0	0	0

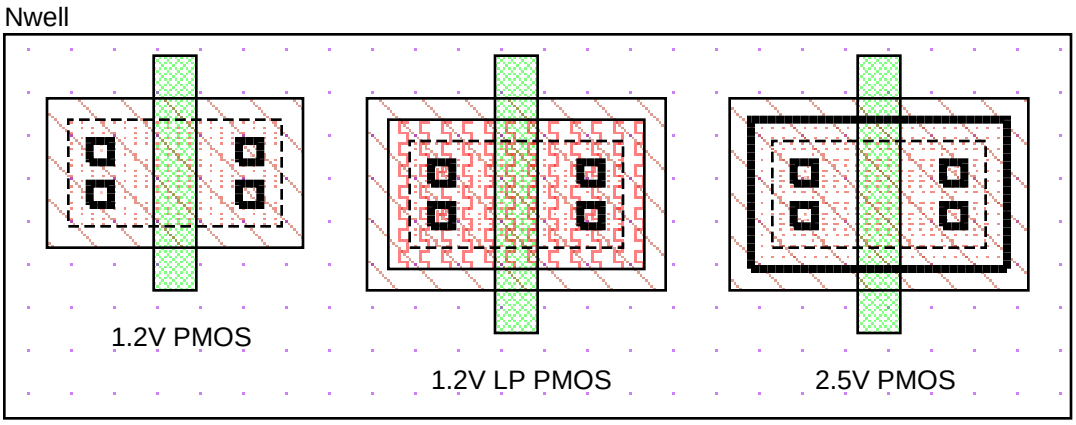
Table 7: Bipolar and Varactor Device Layers

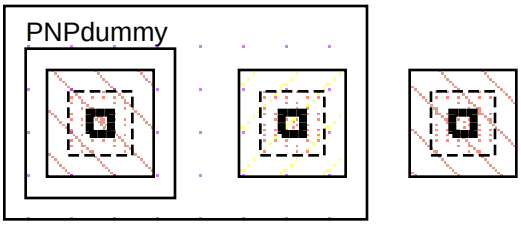
Device Layout Examples

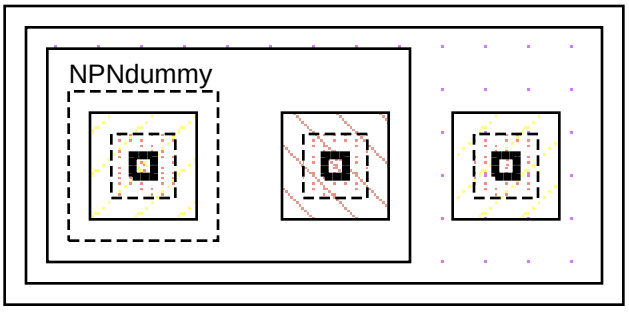


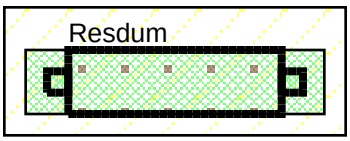




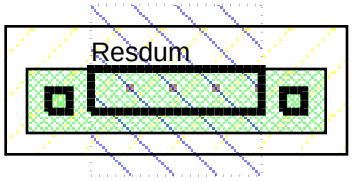




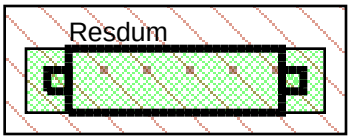




Salicided N+ Poly Resistor



Non-Salicided N+ Poly Resistor



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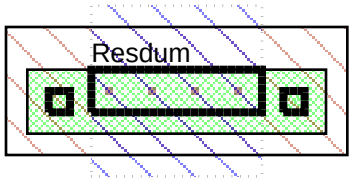
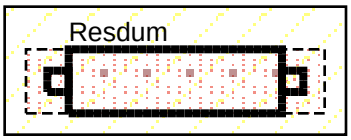
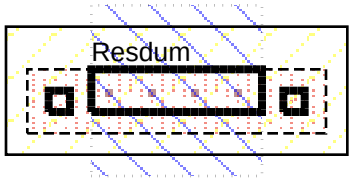


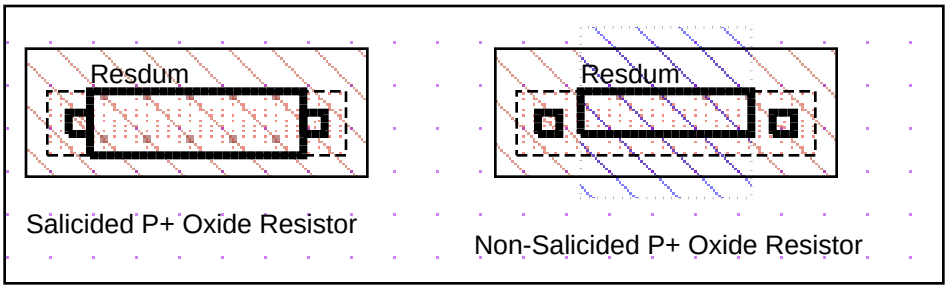
Non-Salicided P+ Poly Resistor



Salicided N+ Oxide Resistor

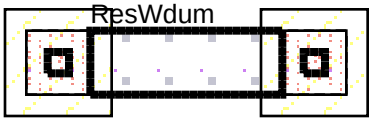


Non-Salicided N+ Oxide Resistor

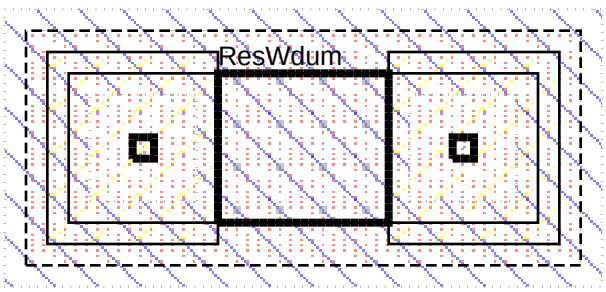


Salicided P+ Oxide Resistor

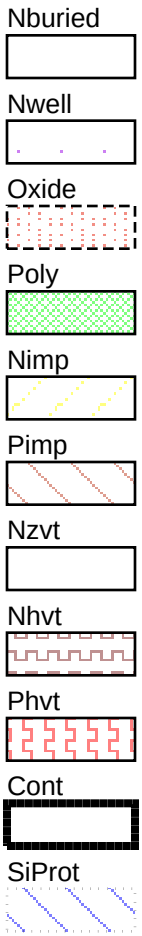
Non-Salicided P+ Oxide Resistor

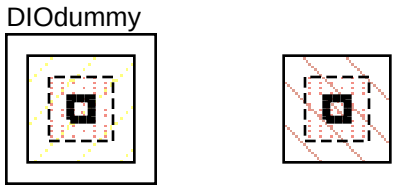


Nwell in STI Resistor

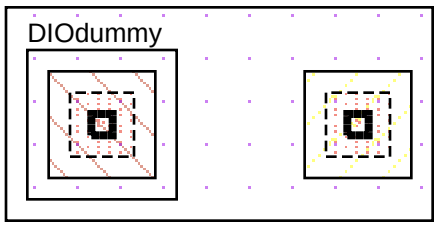


Nwell in OD Resistor

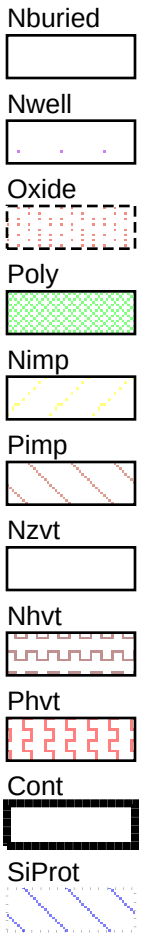




N+/PW Diode



P+/NW Diode

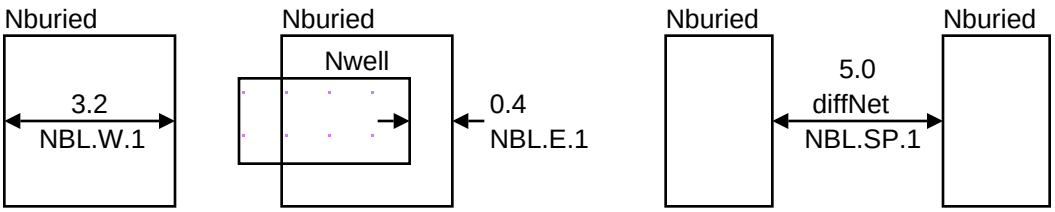


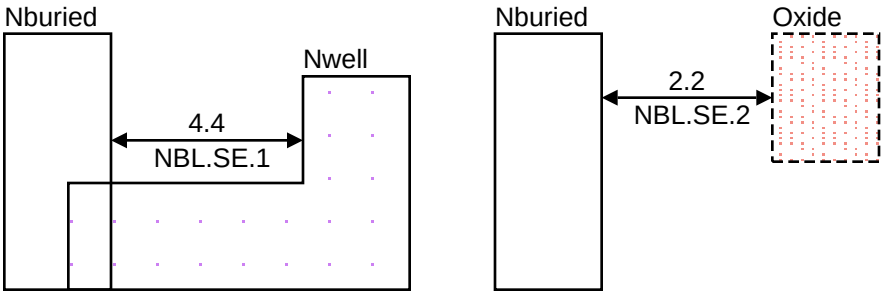
CMOS Digital Core Design Rules

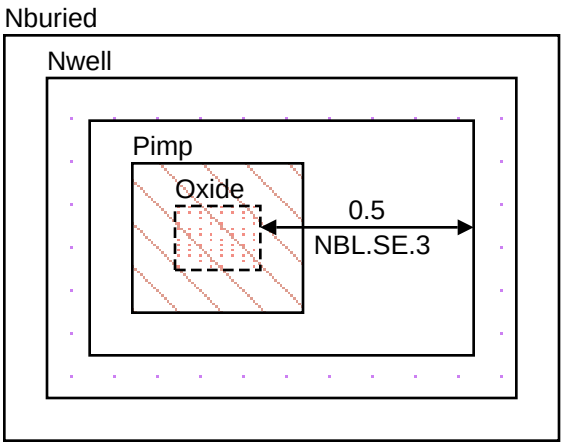
N BURIED LAYER RULES

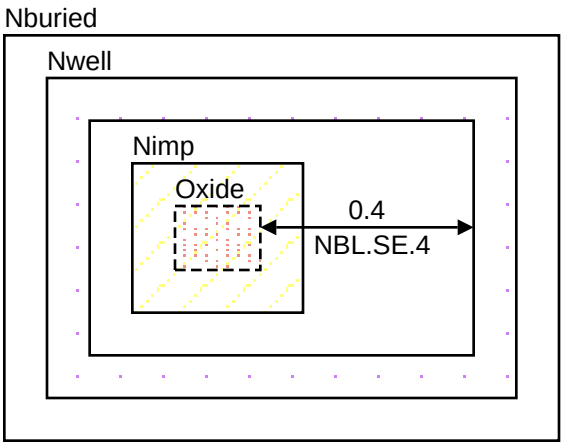
N BURIED LAYER RULES

Rule Name	Value (um)	Description
NBL.W.1	3.2	Minimum Nburied width.
NBL.E.1	0.4	Minimum Nburied to Nwell enclosure.
NBL.SP.1	5.0	Minimum Nburied to Nburied spacing (different potential).
NBL.SE.1	4.4	Minimum Nburied to non-related Nwell spacing.
NBL.SE.2	2.2	Minimum Nburied to Oxide spacing.
NBL.SE.3	0.5	Minimum Nwell ring (on Nburied) to P+ Active Area spacing.
NBL.SE.4	0.4	Minimum Nwell ring (on Nburied) to N+ Active Area spacing.
NBL.X.1	---	Nwell must form isolation rings on Nburied

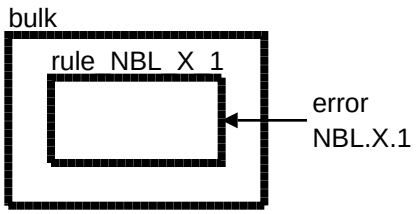








N BURIED LAYER RULES (continued)



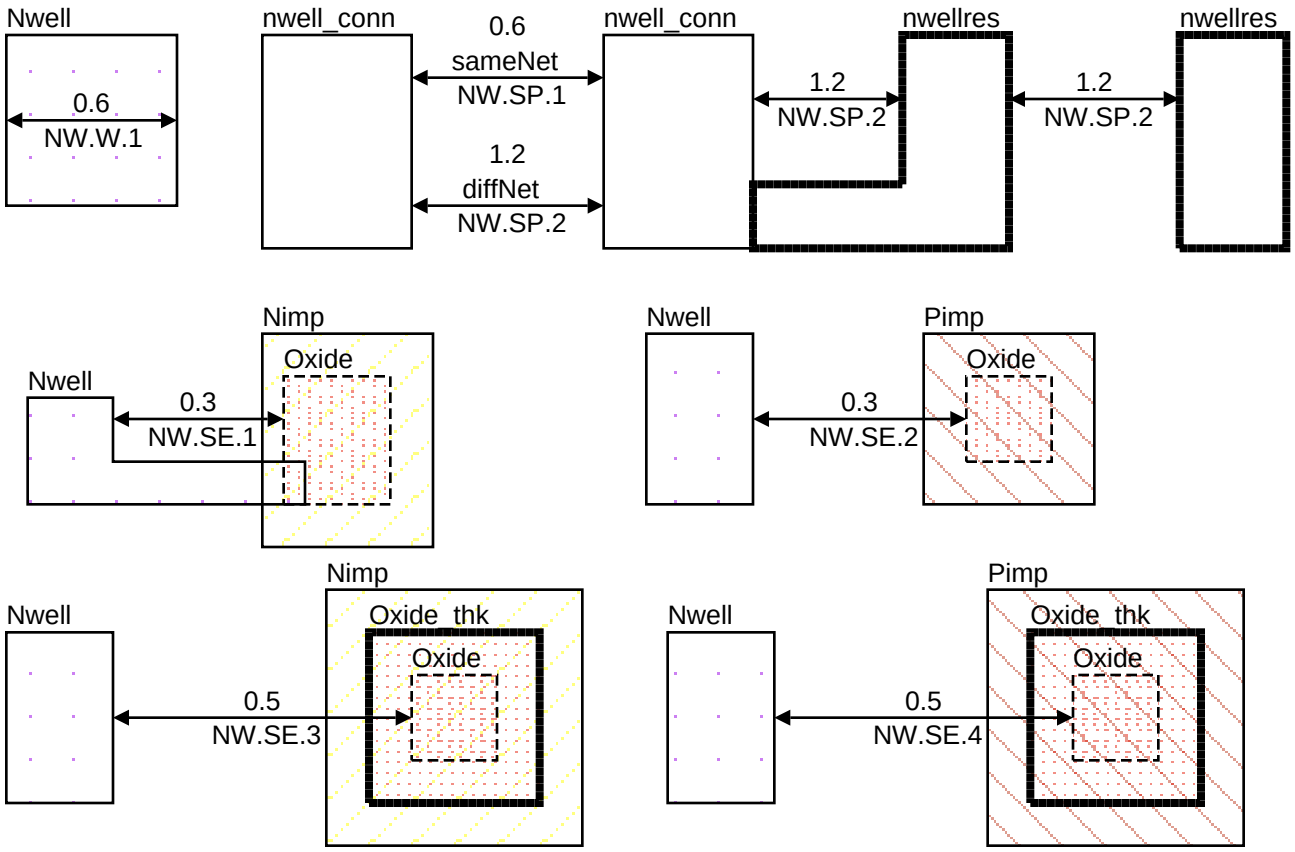
NWELL AND NWELL RESISTOR (under STI) RULES

NWELL AND NWELL RESISTOR (under STI) RULES

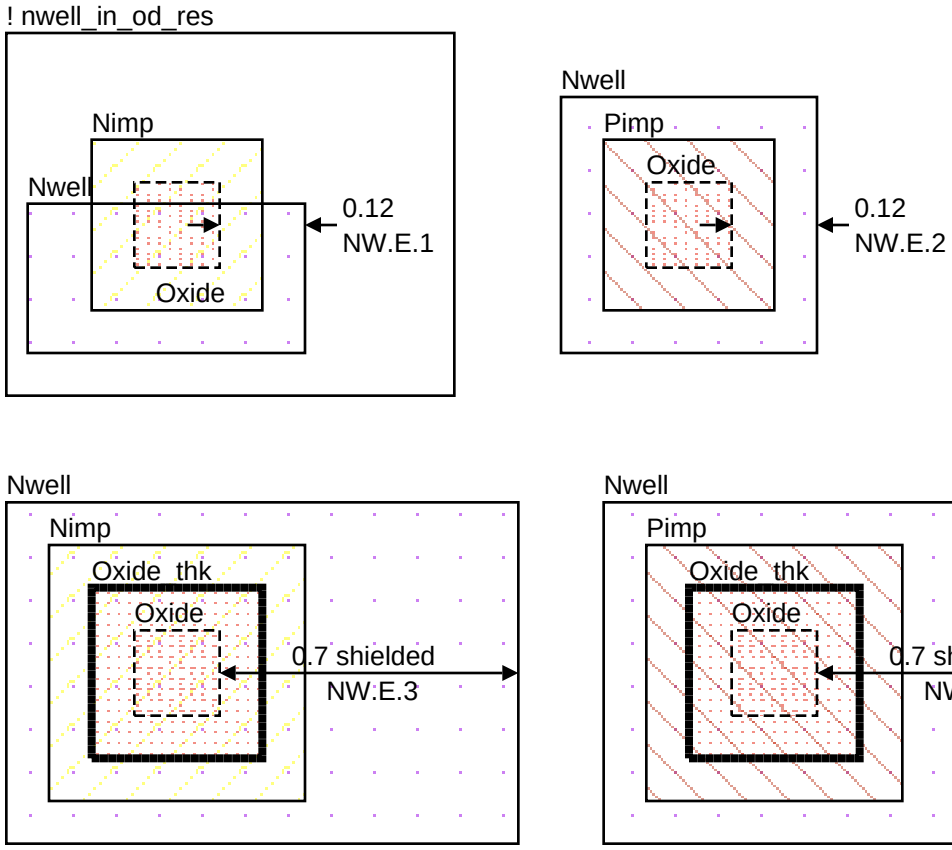
Rule Name	Value (um)	Description
NW.W.1	0.6	Minimum Nwell width.
NW.SP.1	0.6	Minimum Nwell spacing to Nwell (same potential).
NW.SP.2	1.2	Minimum Nwell spacing to Nwell (different potential).
NW.SE.1	0.3	Minimum Nwell spacing to N+ Active Area.
NW.SE.2	0.3	Minimum Nwell spacing to P+ Active Area.
NW.SE.3	0.5	Minimum Nwell spacing to N+ 2.5V Active Area.
NW.SE.4	0.5	Minimum Nwell spacing to P+ 2.5V Active Area.
NW.E.1	0.12	Minimum Nwell enclosure of N+ Active Area.
NW.E.2	0.12	Minimum Nwell enclosure of P+ Active Area.
NW.E.3	0.7	Minimum Nwell enclosure of N+ 2.5V Active Area.
NW.E.4	0.7	Minimum Nwell enclosure of P+ 2.5V Active Area.

Nwell resistor is defined by the intersection of Nwell and ResWdum for DRC and LVS.

For STI Nwell resistors, the ResWdum shape must butt the N+ Oxide on both ends of Nwell the resistor and the ResWdum shape must be coincident or extend beyond the Nwell edges along the length of the Nwell resistor.



NWELL AND NWELL RESISTOR (under STI) RULES (continued)



NWELL RESISTOR WITHIN OXIDE RULES

NWELL RESISTOR WITHIN OXIDE RULES

Rule Name	Value (um)	Description
NWR.E.1	1.2	Minimum Active Area to Nwell (in resistor) enclosure.
NWR.E.2	0.32	Minimum salicided Nwell to Contact enclosure.
NWR.SE.1	0.32	Minimum Resist Protect Oxide to Nwell spacing.
NWR.E.3	0.25	Minimum Resist Protect Oxide to Oxide enclosure.
NWR.O.1	0.45	Minimum N+ Implant to Resist Protect Oxide overlap.
NWR.X.1	---	Thick Oxide is NOT allowed over Nwell resistor.
NWR.SP.1	1.2	Minimum Nwell resistor to other Nwell spacing.

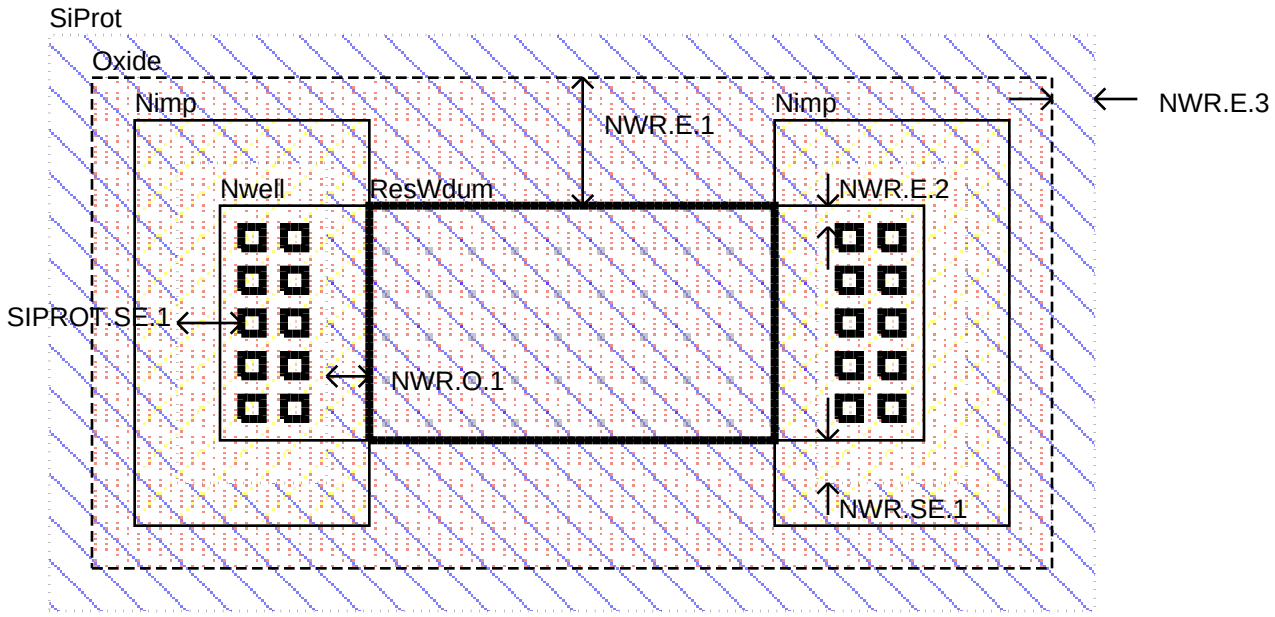
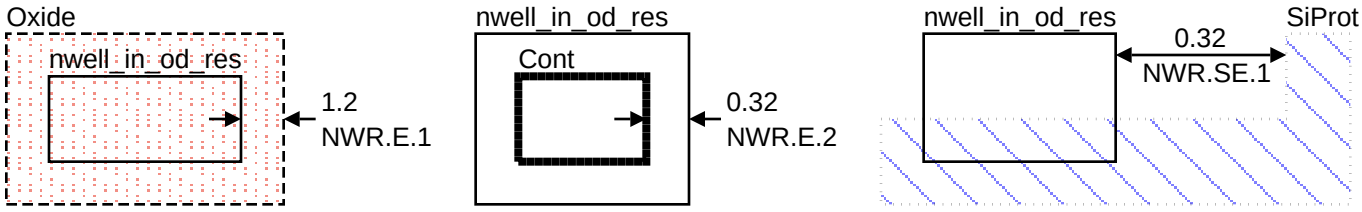


Figure 1: NWELL RESISTOR WITHIN OXIDE RULES

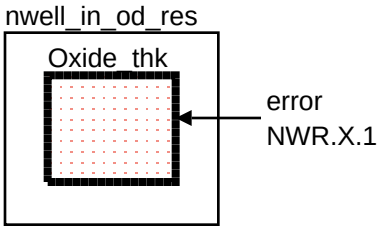
Nwell resistor in Oxide is defined by the intersection of Nwell and Resdum for DRC and LVS.

For Nwell resistor within Oxide, the ResWdum shape must butt the Nimp on both ends of the Nwell resistor and the ResWdum shape must be coincident or extend beyond the Nwell edges along the length of the Nwell resistor.



NWELL RESISTOR WITHIN OXIDE RULES (continued)

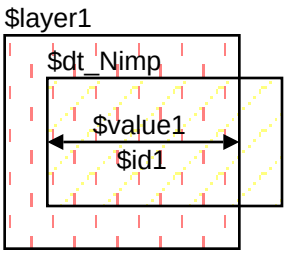
NWR.E.3 - Covered by SIPROT.E.1.



NWR.SP.1 - Covered by NW.SP.2.

SiProt/Nimp Overlap Check - with context

macro



Macro Table

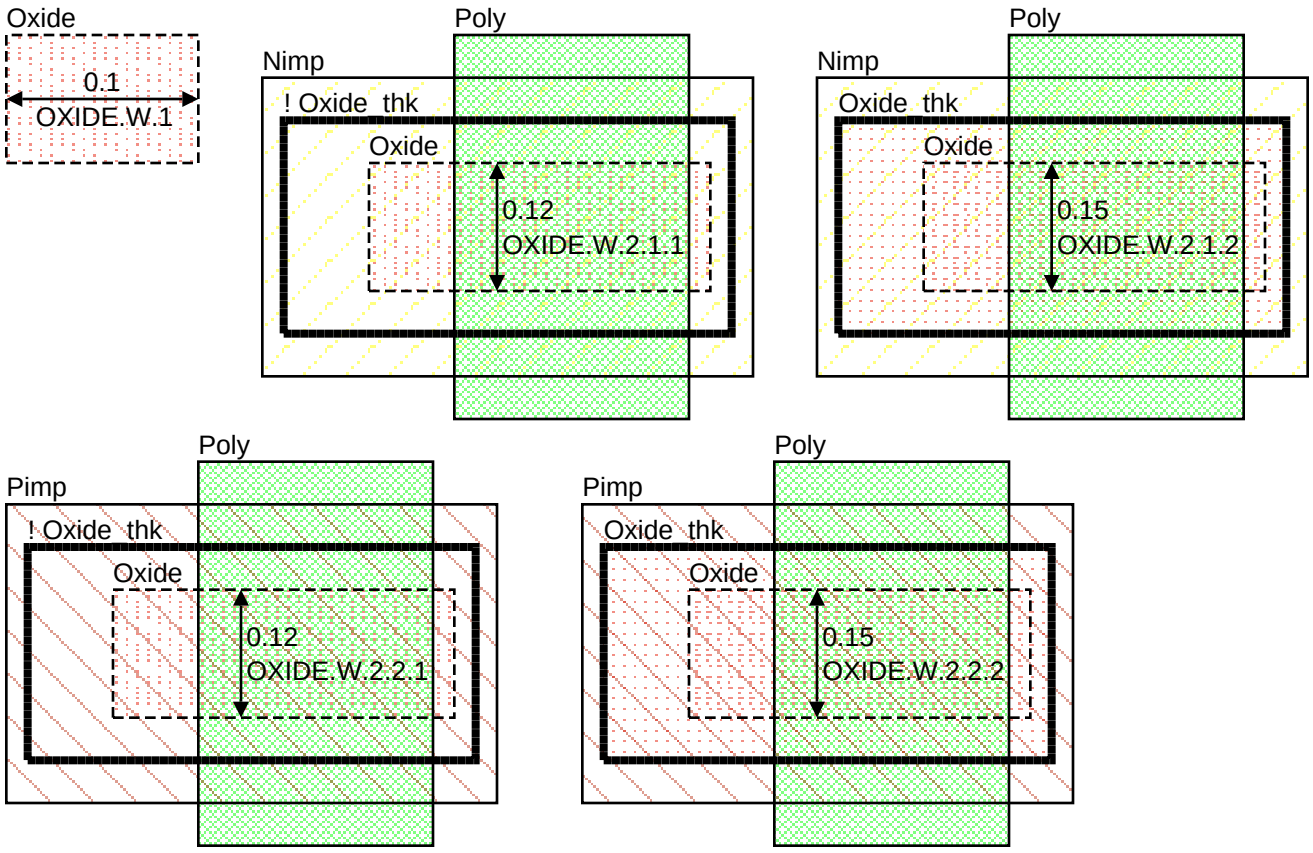
$layer1	$dt_Nimp	$id1	$value1
siprot_in_nwell_res	Nimp	NWR.O.1	0.45

$message1
SiProt to Nimp overlap must be >= 0.45 um

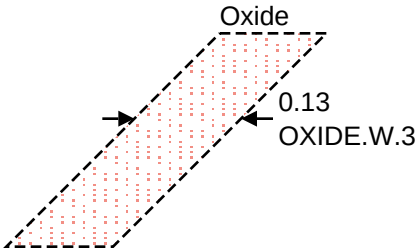
ACTIVE RULES

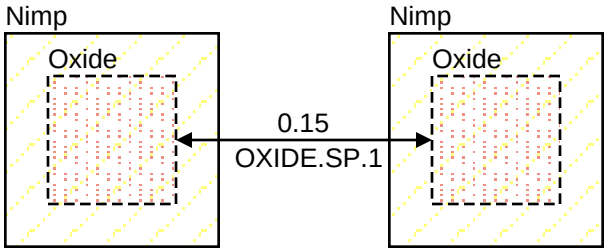
ACTIVE RULES

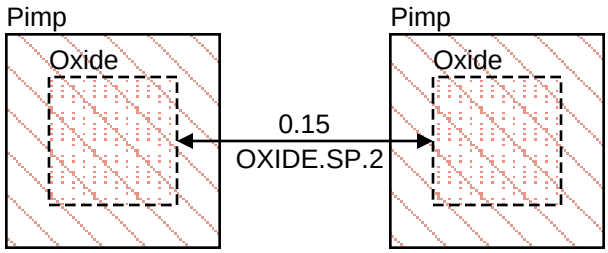
Rule Name	Value (um)	Description
OXIDE.W.1	0.1	Minimum Active Area width.
OXIDE.W.2.1.1	0.12	Minimum 1.2V N-channel gate width.
OXIDE.W.2.1.2	0.15	Minimum 2.5V N-channel gate width.
OXIDE.W.2.2.1	0.12	Minimum 1.2V P-channel gate width.
OXIDE.W.2.2.2	0.15	Minimum 2.5V P-channel gate width.
OXIDE.W.3	0.13	Minimum Active Area bent 45 degrees width.
OXIDE.SP.1	0.15	Minimum N+ Active Area to N+ Active Area spacing.
OXIDE.SP.2	0.15	Minimum P+ Active Area to P+ Active Area spacing.
OXIDE.SP.3	0.15	Minimum N+ Active Area to P+ Active Area spacing.
OXIDE.SP.4	0.18	Minimum Active Area bent 45 degrees to Active Area spacing.
OXIDE.SE.1	0.28	Minimum Active Area to Thick Active Area spacing.
OXIDE.A.1	0.06	Minimum area fpr Active Area.
OXIDE.EA.1	0.1	Minimum Active Area enclosed area ("donut" hole surrounded by Active Area).
OXIDE.L.1	22.0	Maximum Oxide length between two contacts when the Oxide width is <= 0.18um.
OXIDE.L.2	11.0	Maximum Oxide length between one contact and the end of the Oxide line when the Oxide width is <= 0.18um.
OXIDE.X.1	---	Oxide must be covered by N+ Implant or P+ Implant or Nzvt or Salicide Block.

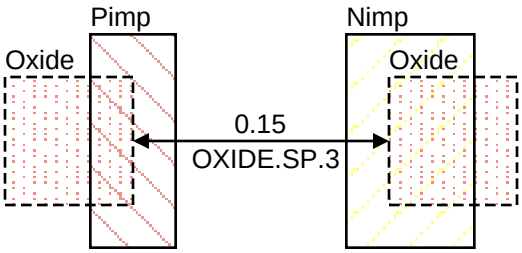


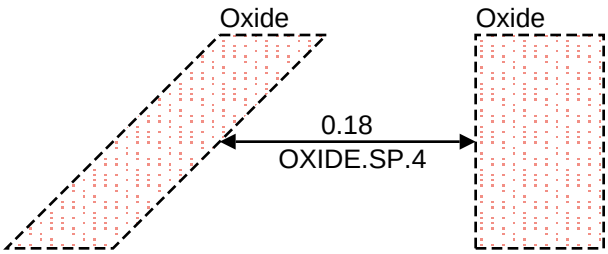
ACTIVE RULES (continued)

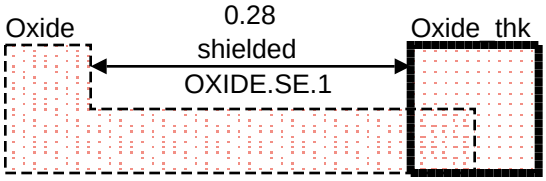


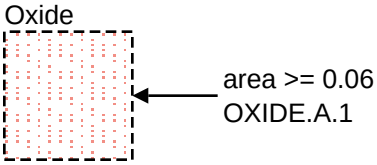


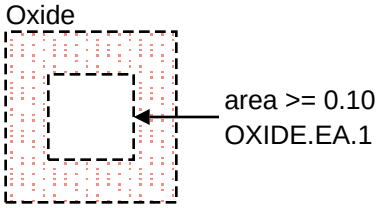


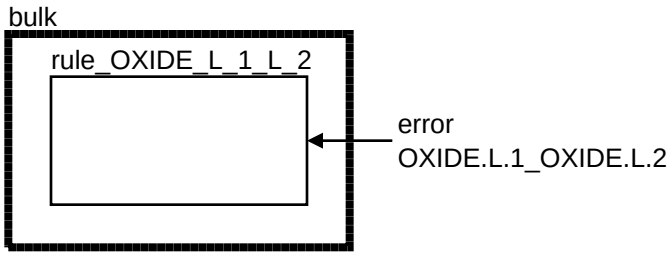


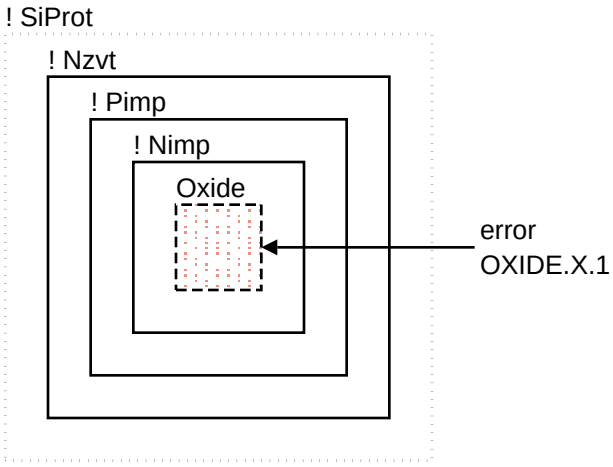












ACTIVE RESISTOR RULES (salicided/non-salicided)

ACTIVE RESISTOR RULES (salicided/non-salicided)

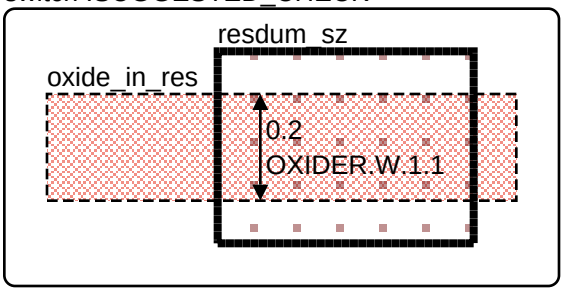
Rule Name	Value (um)	Description
OXIDER.W.1.1	0.2	Minimum Active resistor width.
OXIDER.W.1.2	1.5	Minimum suggested Active resistor width.
OXIDER.L.1	8.0	Minimum suggested Active resistor length.
OXIDER.SE.1	0.25	Minimum Salicide Block to Contact spacing.
OXIDER.E.1	0.25	Minimum Salicide Block to Active resistor enclosure.
OXIDER.SE.2	0.3	Minimum Active resistor to N+ or P+ Implant spacing.
OXIDER.X.1	---	Active resistors must have N+ or P+ Implant.

Active resistor is defined by the intersection of Oxide and Resdum for DRC and LVS.

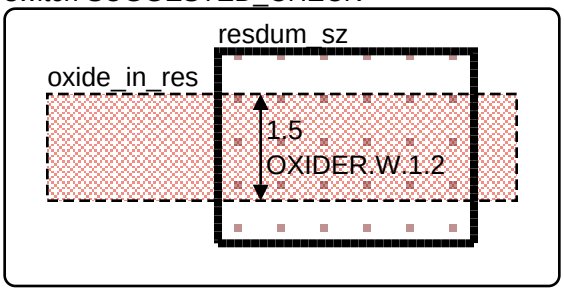
For salicided Oxide resistors, the Resdum shape must butt the contacts on both ends of Oxide the resistor and the Resdum shape must be coincident or extend beyond the Oxide edges along the length of the Oxide resistor.

For non-salicided Oxide resistors, the Resdum shape must be coincident with the edges of the Siprot that crosses the width of the Oxide resistor and the Resdum shape must be coincident or extend beyond the Oxide edges along the length of the Oxide resistor.

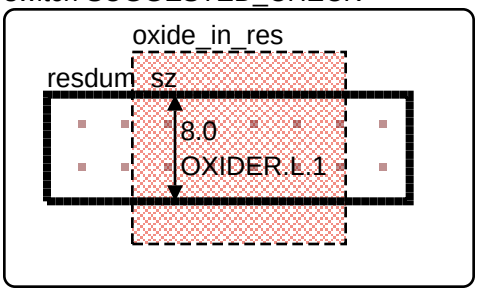
switch !SUGGESTED_CHECK

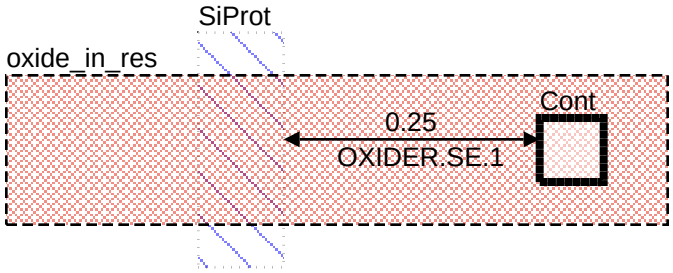


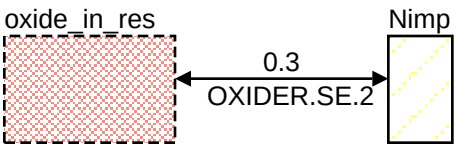
switch SUGGESTED_CHECK

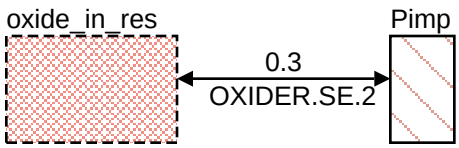


switch SUGGESTED_CHECK

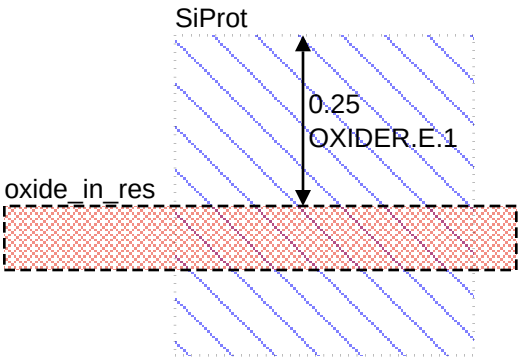


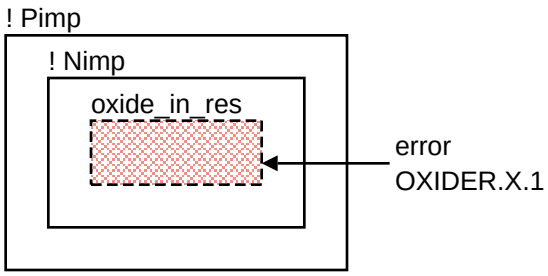






ACTIVE RESISTOR RULES (continued)



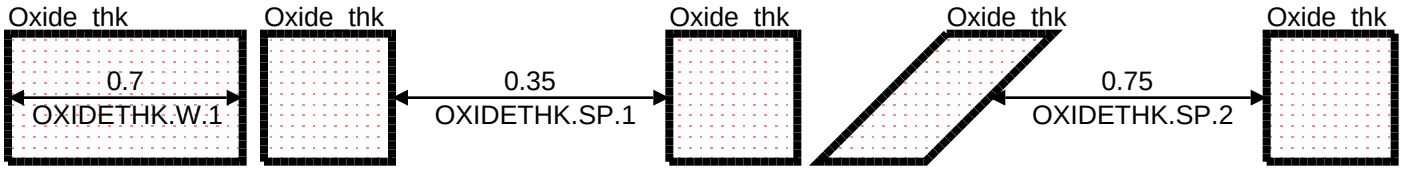


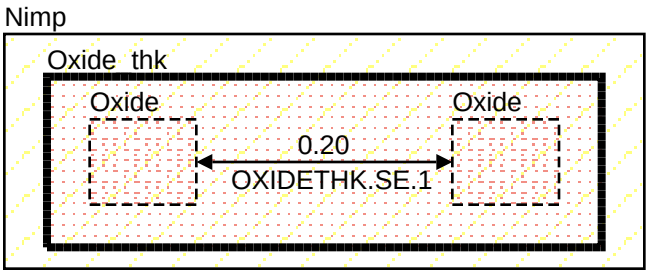
THICK ACTIVE (2.5V) RULES

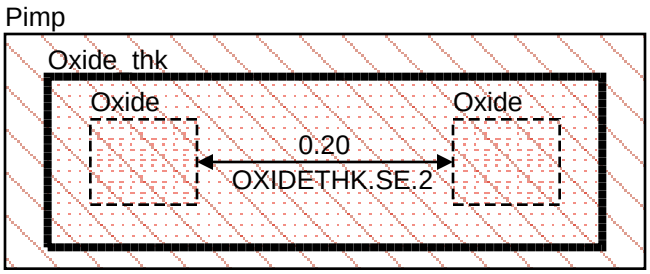
THICK ACTIVE (2.5V) RULES

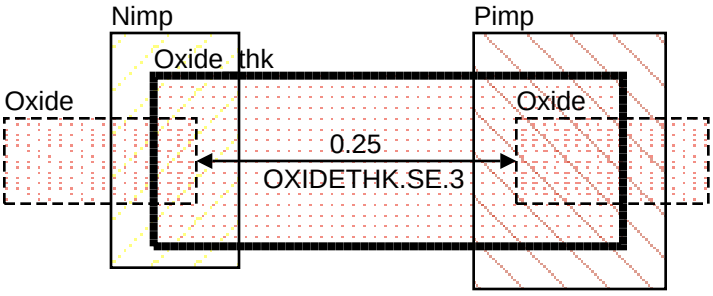
Rule Name	Value (um)	Description
OXIDETHK.W.1	0.7	Minimum Thick Active Area width.
OXIDETHK.SP.1	0.35	Minimum Thick Active Area to Thick Active Area spacing.
OXIDETHK.SP.2	0.75	Minimum Thick Active Area bent 45 degrees to Thick Active Area spacing.
OXIDETHK.SE.1	0.20	Minimum N+ 2.5V Active Area to 2.5V N+ Active Area spacing.
OXIDETHK.SE.2	0.20	Minimum P+ 2.5V Active Area to 2.5V P+ Active Area spacing.
OXIDETHK.SE.3	0.25	Minimum N+ 2.5V Active Area to 2.5V P+ Active Area spacing.
OXIDETHK.SE.4	0.28	Minimum Thick Active Area to Active Area spacing.
OXIDETHK.E.1	0.3	Minimum Thick Active Area to Active Area enclosure.
OXIDETHK.SE.5	0.34	Minimum Thick Active Area to 1.2V Poly gate spacing.
OXIDETHK.E.2	0.36	Minimum Thick Active Area to Thick Poly gate enclosure.

Note 1: 2.5V MOS must be defined by Active which is fully enclosed by Thick Active (with 0.0 overlap).
Note 2: 1.2V MOS is only defined by Active without any Thick Active.



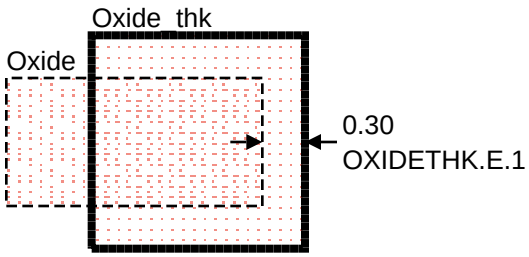


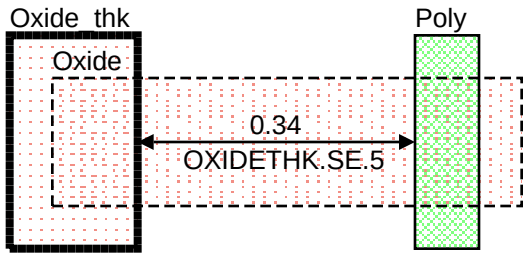


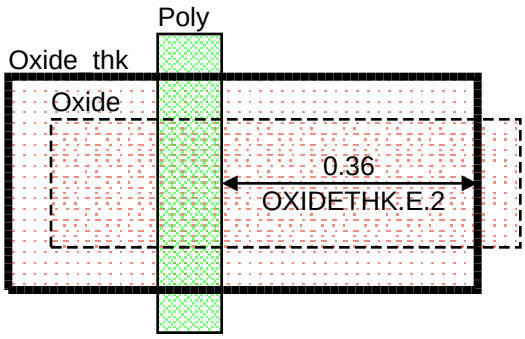


OXIDETHK.SE.4 - Covered by OXIDE.SE.1.

Thick ACTIVE RULES (continued)





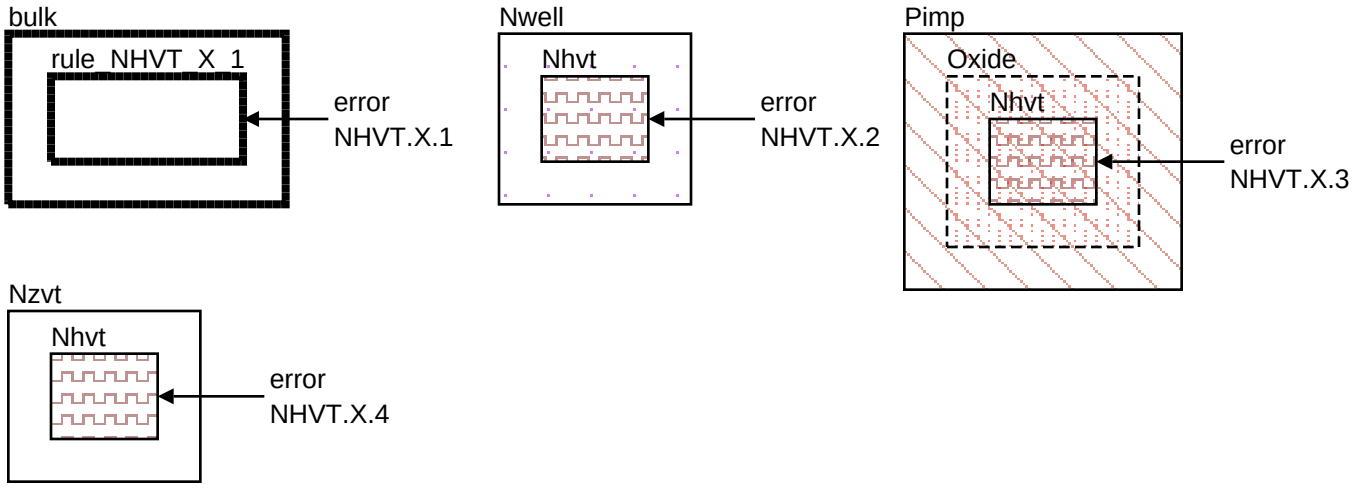


N+ HIGH VT RULES

N+ HIGH VT RULES RULES

Rule Name	Value (um)	Description
NHVT.X.1	---	Nhvt exactly matches the Oxide it is on (0.0 enclosure on all sides).
NHVT.X.2	---	Nhvt is NOT allowed on Nwell.
NHVT.X.3	---	Nhvt is NOT allowed on P+ Active.
NHVT.X.4	---	Nhvt is NOT allowed on Nzvt.

Note 1: Nhvt defines the 1.2V LP NMOS device.

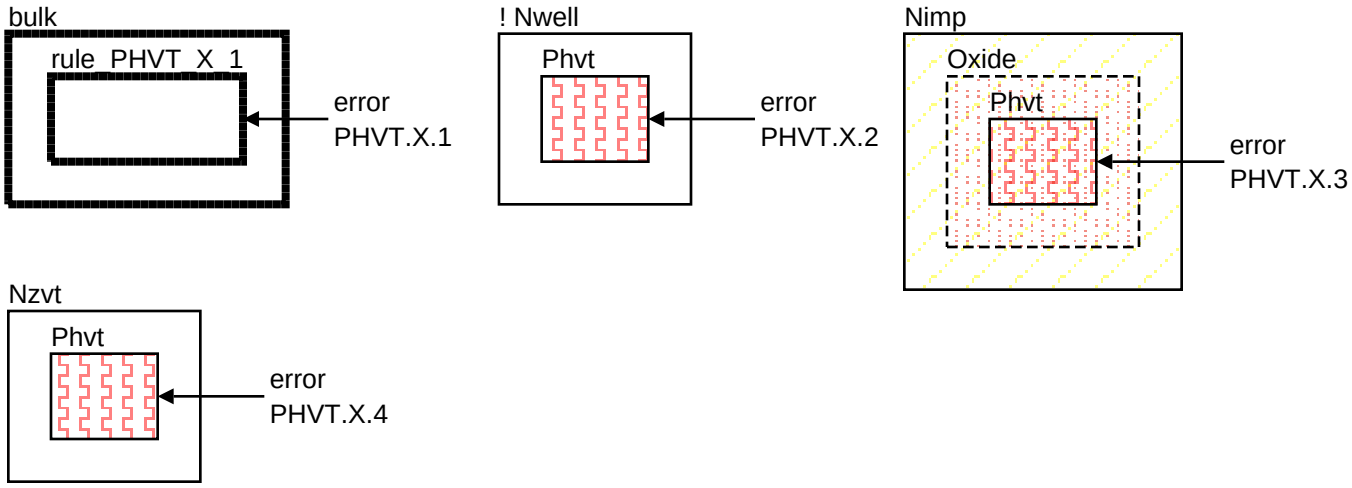


P+ HIGH VT RULES

P+ HIGH VT RULES RULES

Rule Name	Value (um)	Description
PHVT.X.1	---	Phvt exactly matches the Oxide it is on (0.0 enclosure on all sides).
PHVT.X.2	---	Phvt is NOT allowed outside Nwell.
PHVT.X.3	---	Phvt is NOT allowed on N+ Active.
PHVT.X.4	---	Phvt is NOT allowed on Nzvt.

Note 1: Phvt defines the 1.2V LP PMOS device.

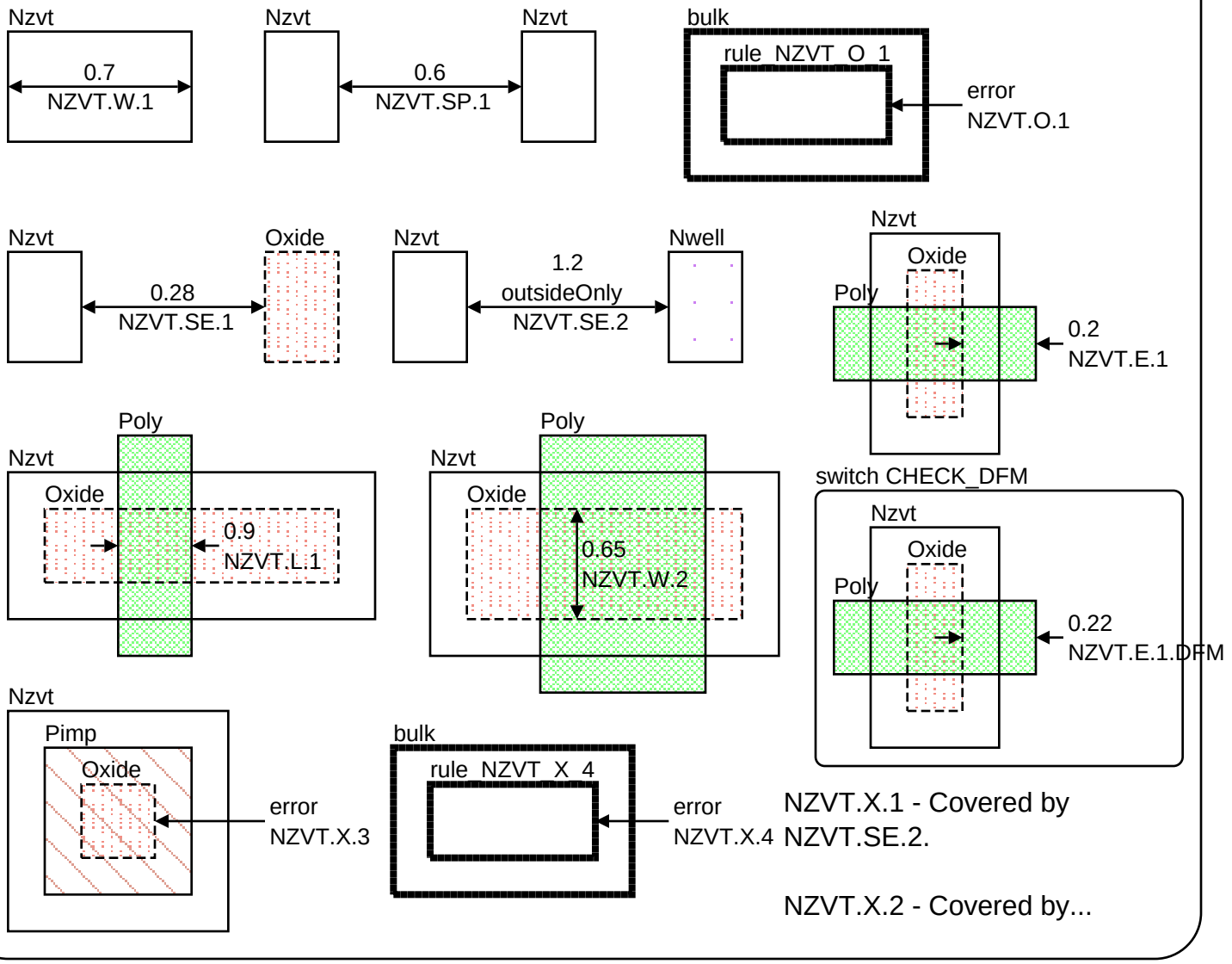


NATIVE NMOS ACTIVE RULES

NATIVE NMOS ACTIVE RULES

Rule Name	Value (um)	Description
NZVT.W.1	0.7	Minimum Nzvt width.
NZVT.SP.1	0.6	Minimum Nzvt to Nzvt spacing.
NZVT.O.1	0.3	Minimum and maximum Nzvt to Active Area overlap.
NZVT.SE.1	0.28	Minimum Nzvt to Active spacing.
NZVT.SE.2	1.2	Minimum Nzvt to Nwell spacing.
NZVT.E.1	0.2	Minimum N+ Poly gate end cap to Native Active Area enclosure.
NZVT.E.1.DFM	0.22	Minimum N+ Poly gate end cap to Native Active Area enclosure for DFM.
NZVT.L.1	0.9	Minimum Native device Poly gate length.
NZVT.W.2	0.65	Minimum Native device Poly gate width.
NZVT.X.1	---	Nzvt is NOT allowed on Nwell.
NZVT.X.2	---	Bent Poly gates are NOT allowed on Nzvt.
NZVT.X.3	---	P+ Active Area is NOT allowed on Nzvt.
NZVT.X.4	---	Only one Active Area is allowed in an Nzvt region.

Note 1: Native NMOS is defined by Active which is full enclosed by Nzvt with 0.3um enclosure.



NZVT.X.1 - Covered by NZVT.SE.2.

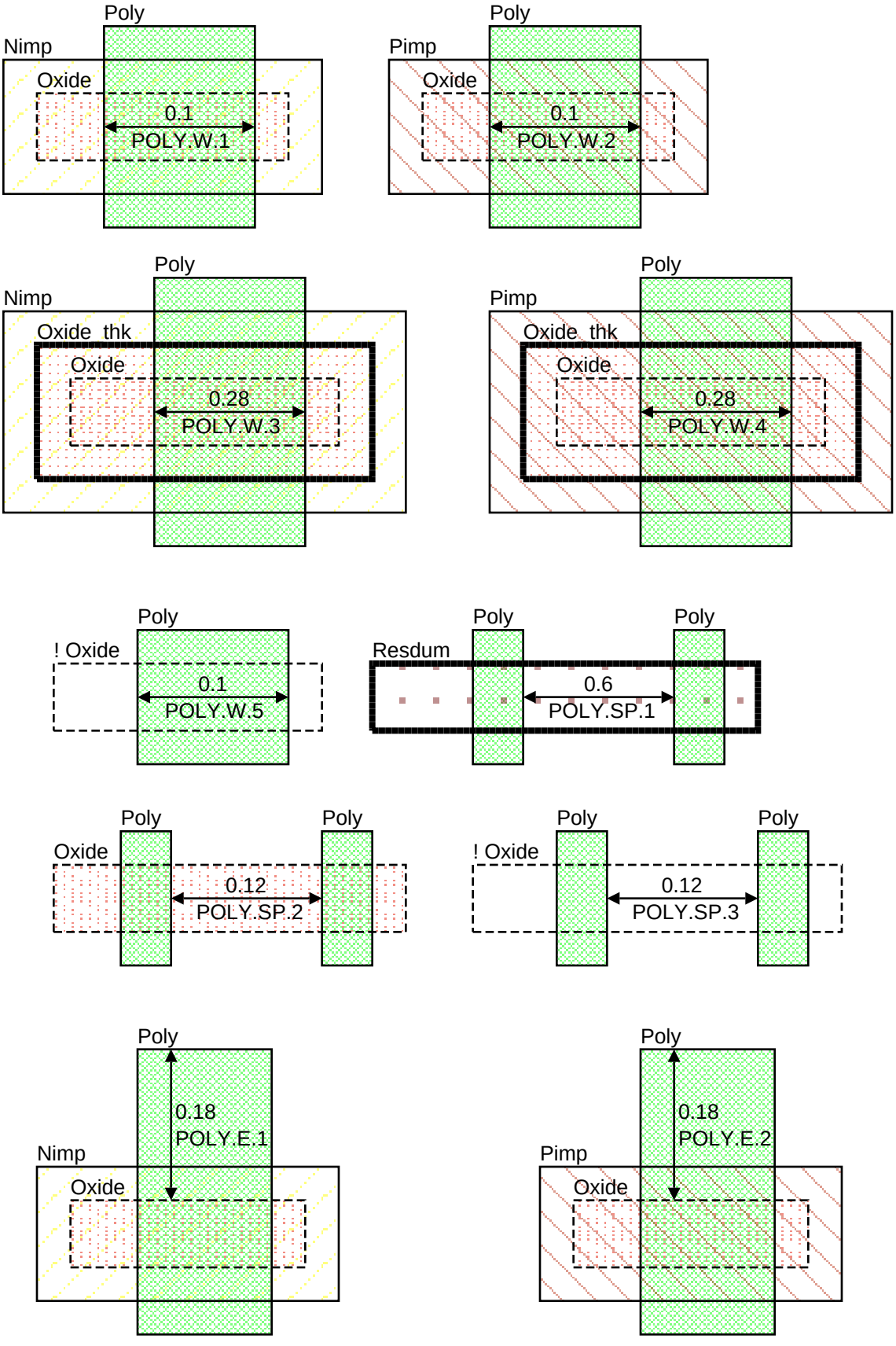
NZVT.X.2 - Covered by...

POLY RULES

POLY RULES

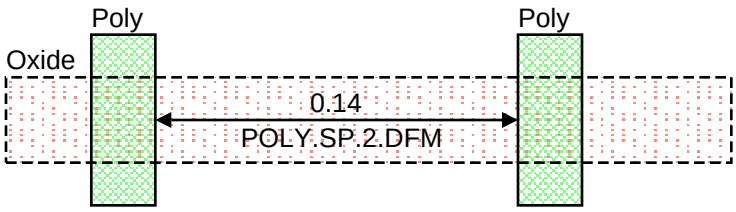
Rule Name	Value (um)	Description
POLY.W.1	0.1	Minimum 1.2V N-channel gate length.
POLY.W.2	0.1	Minimum 1.2V P-channel gate length.
POLY.W.3	0.28	Minimum 2.5V N-channel gate length.
POLY.W.4	0.28	Minimum 2.5V P-channel gate length.
POLY.W.5	0.1	Minimum Poly interconnect width.
POLY.SP.1	0.6	Minimum Poly resistor space.
POLY.SP.2	0.12	Minimum gate space.
POLY.SP.2.DFM	0.14	Minimum gate space for DFM.
POLY.SP.3	0.12	Minimum Poly interconnect space.
POLY.E.1	0.18	Minimum N-channel gate extension beyond Active Area.
POLY.E.2	0.18	Minimum P-channel gate extension beyond Active Area.
POLY.E.1.DFM	0.20	Minimum N-channel gate extension beyond Active Area for DFM.
POLY.E.2.DFM	0.20	Minimum P-channel gate extension beyond Active Area for DFM.
POLY.SE.1	0.1	Minimum Poly interconnect to unrelated Active Area space.
POLY.SE.2	0.1	Minimum Poly interconnect to related Active Area space.
POLY.E.3	0.2	Minimum Active Area (source/drain) to gate enclosure.
POLY.W.6	0.18	Minimum bent Poly width.
POLY.SP.4	0.22	Minimum bent Poly space.
POLY.X.1	***	Bent gate is not allowed.
POLY.X.2	***	Bent Poly resistor is not allowed.
POLY.D.1	50%	Maximum Poly density across full chip.
POLY.SE.3	25	Maximum Poly segment length (width < 0.14) between two contacts.
POLY.A.1	0.1	Minimum area for Poly interconnect.

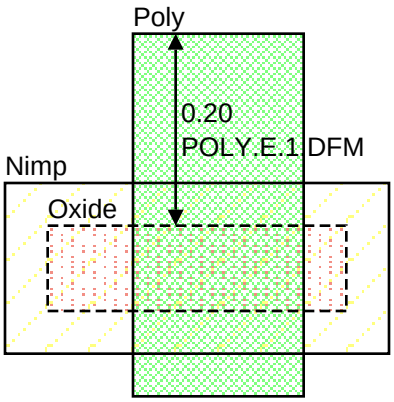
POLY RULES (continued)

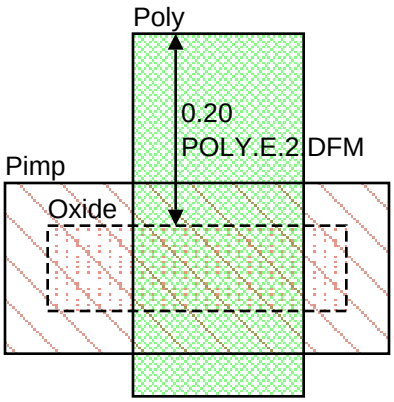


POLY RULES (continued)

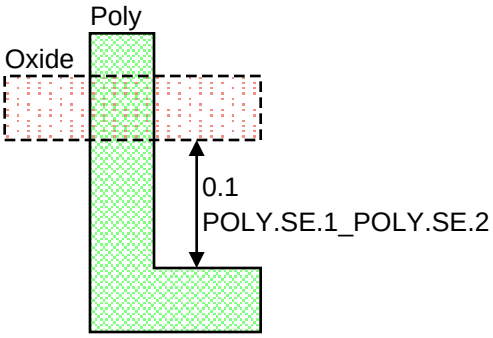
switch CHECK_DFM

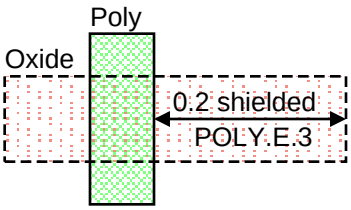


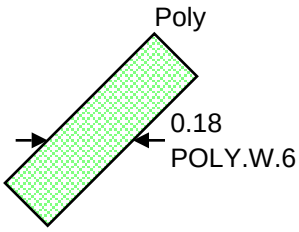


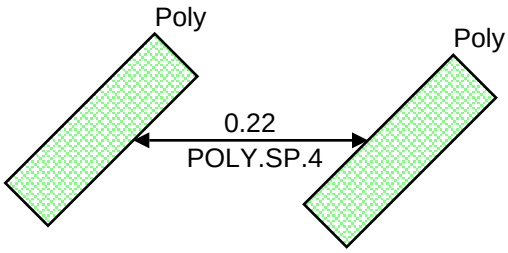


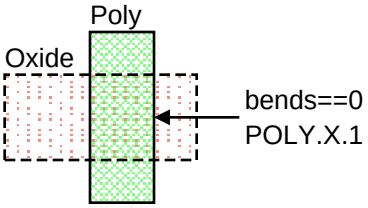
POLY RULES (continued)

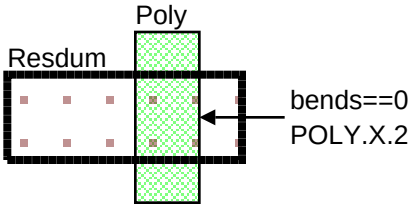


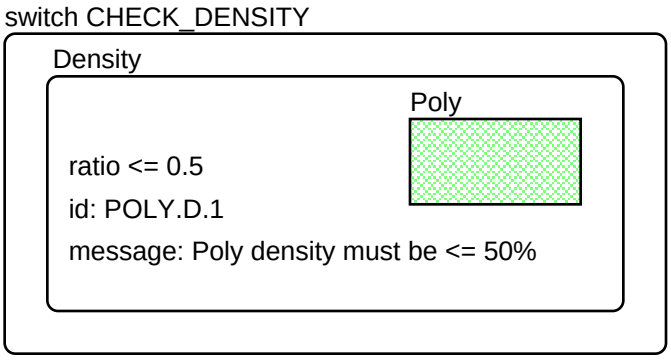


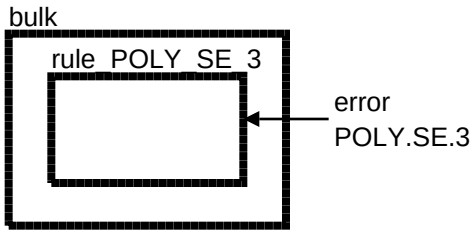


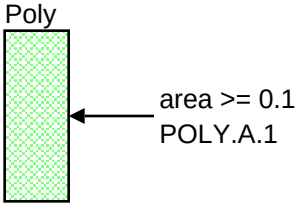












POLY RESISTOR RULES (salicided/non-salicided)

POLY RESISTOR RULES (salicided/non-salicided)

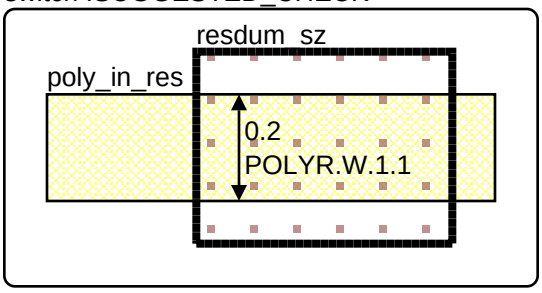
Rule Name	Value (um)	Description
POLYR.W.1.1	0.2	Minimum Poly resistor width.
POLYR.W.1.2	1.5	Minimum suggested Poly resistor width.
POLYR.L.1	8.0	Minimum suggested Poly resistor length.
POLYR.SE.1	0.25	Minimum Salicide Block to Contact spacing.
POLYR.E.1	0.28	Minimum Salicide Block to Poly resistor enclosure.
POLYR.E.2	0.15	Minimum N+ Implant to Poly used in resistor enclosure.
POLYR.E.3	0.15	Minimum P+ Implant to Poly used in resistor enclosure.
POLYR.SE.2	0.3	Minimum Poly resistor to other Implant spacing.
POLYR.X.1	---	Poly resistors must have N+ or P+ Implant.

Poly resistor is defined by the intersection of Poly and Resdum for DRC and LVS.

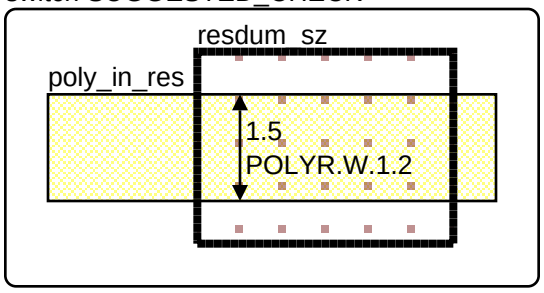
For salicided Poly resistors, the Resdum shape must butt the contacts on both ends of Poly the resistor and the Resdum shape must be coincident or extend beyond the Poly edges along the length of the Poly resistor.

For non-salicided Poly resistors, the Resdum shape must be coincident with the edges of the Siprot that crosses the width of the Poly resistor and the Resdum shape must be coincident or extend beyond the Poly edges along the length of the Poly resistor.

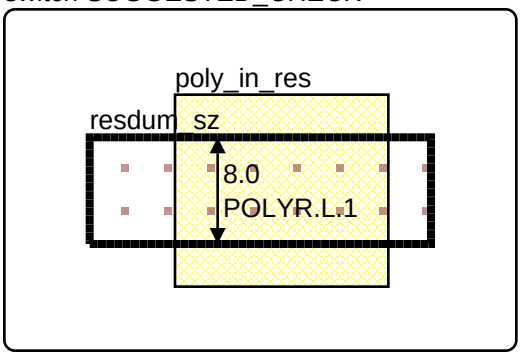
switch !SUGGESTED_CHECK

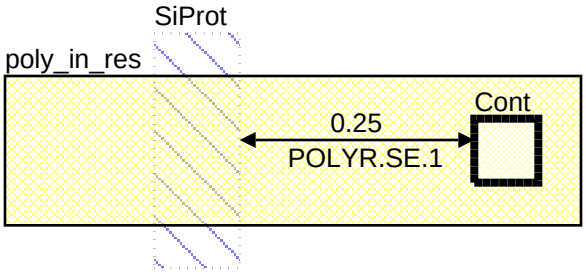


switch SUGGESTED_CHECK

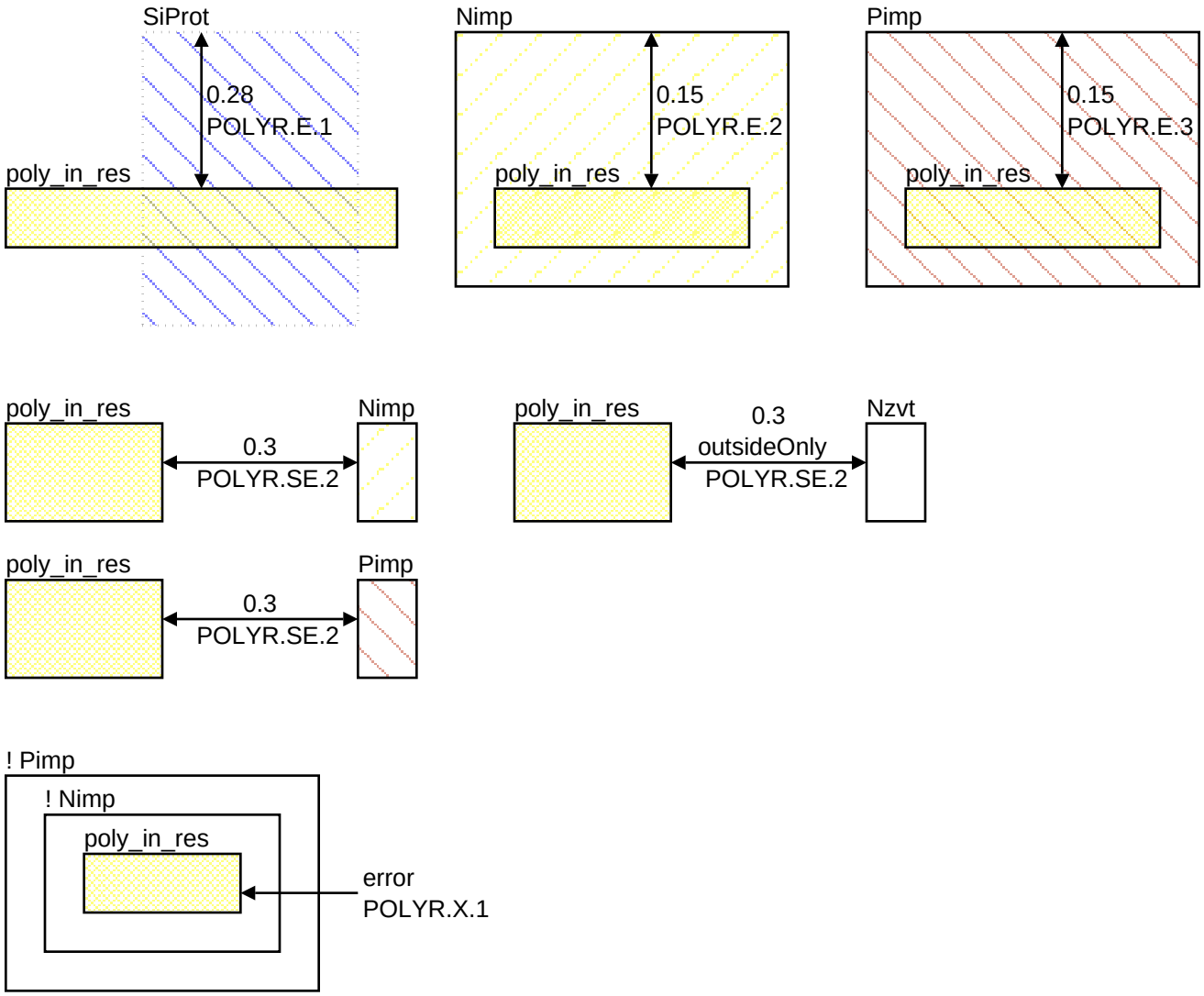


switch SUGGESTED_CHECK





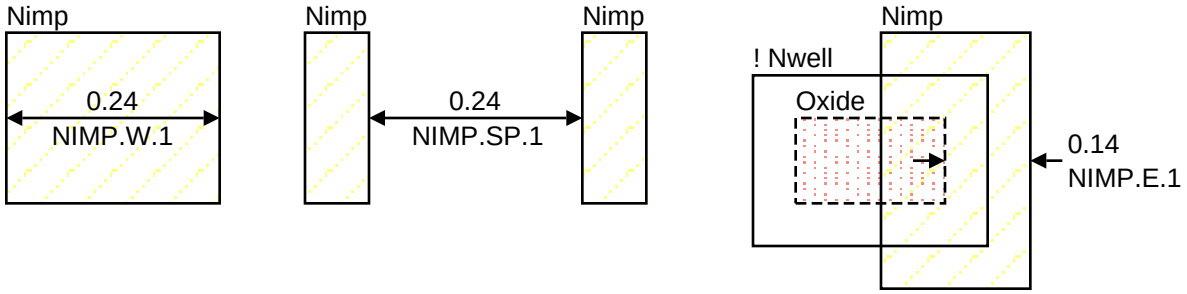
POLY RESISTOR RULES (continued)

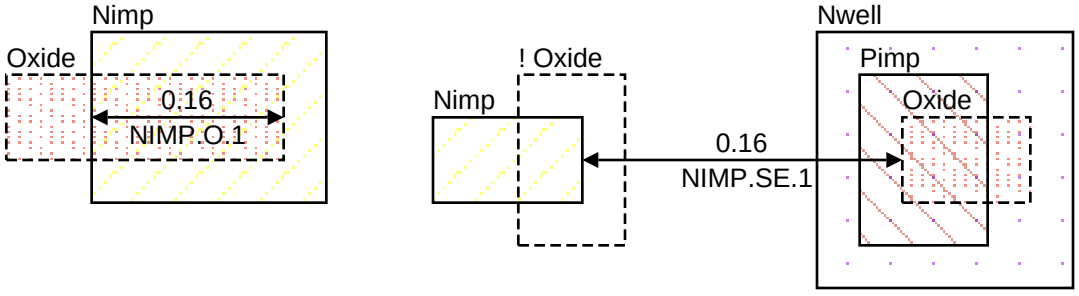


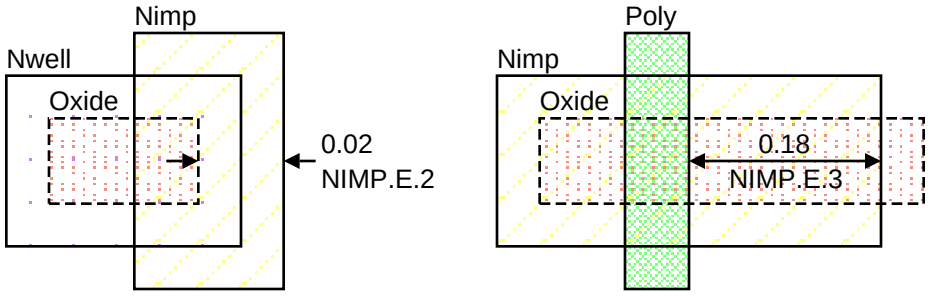
N+ IMPLANT RULES

N+ IMPLANT RULES

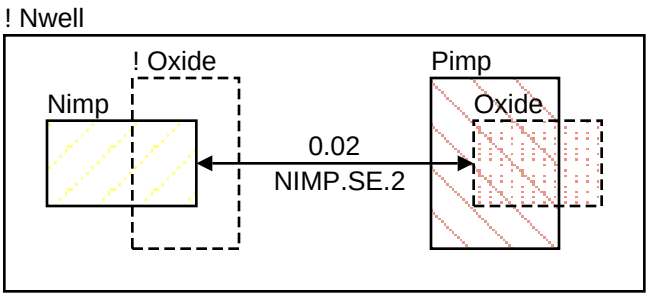
Rule Name	Value (um)	Description
NIMP.W.1	0.24	Minimum N+ Implant width.
NIMP.SP.1	0.24	Minimum N+ Implant space.
NIMP.E.1	0.14	Minimum N+ Implant to Active Area enclosure.
NIMP.O.1	0.16	Minimum N+ Implant to Active Area overlap.
NIMP.SE.1	0.16	Minimum N+ Implant to P+ Active (inside Nwell) Area spacing.
NIMP.E.2	0.02	Minimum N+ Implant to Active Area (Nwell tie) enclosure.
NIMP.E.3	0.18	Minimum N+ Implant to gate side enclosure.
NIMP.SE.2	0.02	Minimum N+ Implant to P+ Active Area (substrate tie) spacing.
NIMP.E.4	0.18	Minimum N+ to gate (endcap) enclosure.
NIMP.SE.3	0.18	Minimum N+ Implant to P+ gate side (butted Implant) spacing.
NIMP.A.1	0.15	Minimum area for N+ Implant.
NIMP.EA.1	0.16	Minimum N+ Implant ring enclosed area ("donut" hole surrounded by N+ Implant).
NIMP.X.1	---	N+ Implant is NOT allowed over P+ Implant.

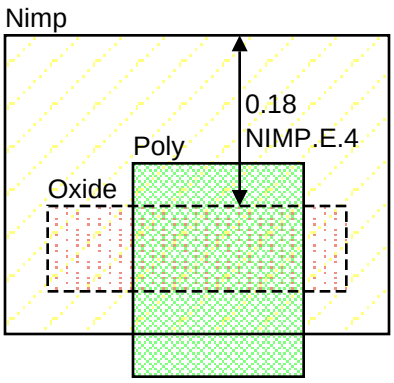


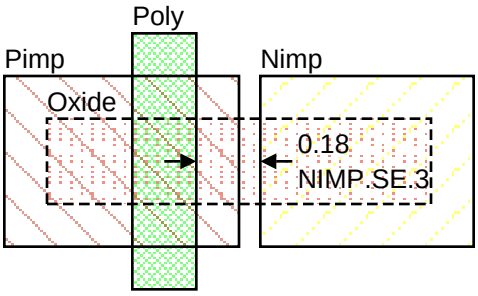


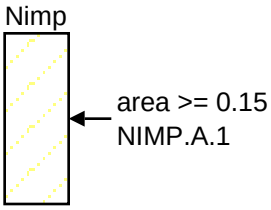


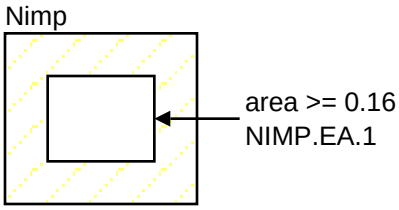
N+ IMPLANT RULES (continued)

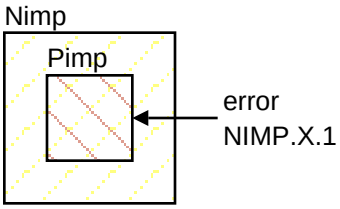








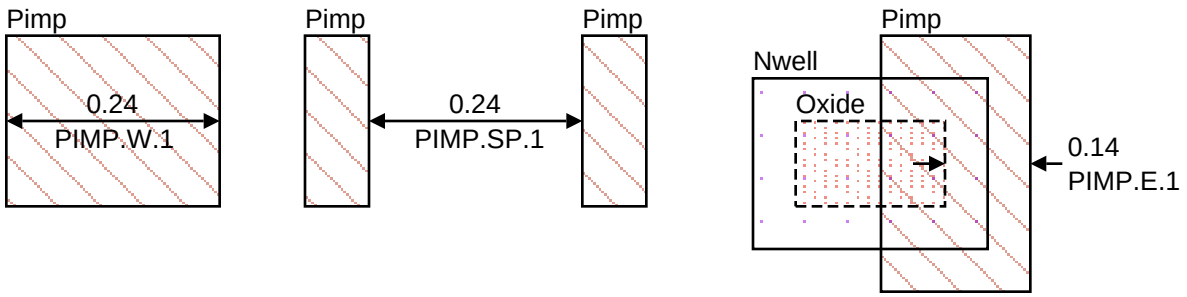


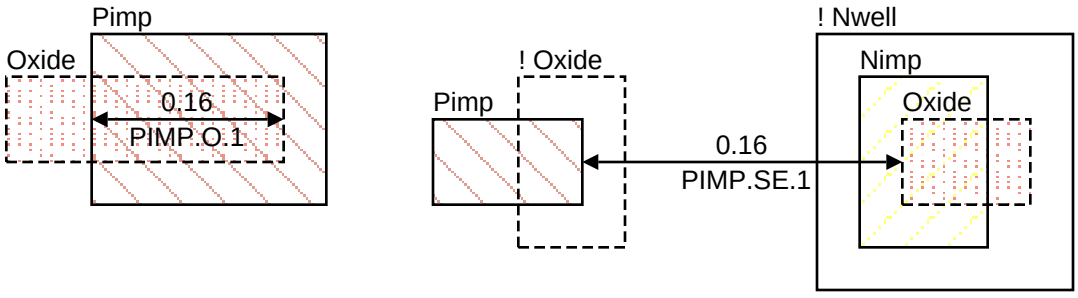


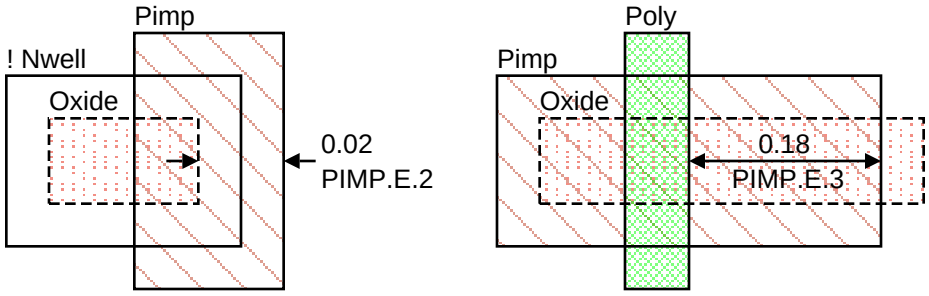
P+ IMPLANT RULES

P+ IMPLANT RULES

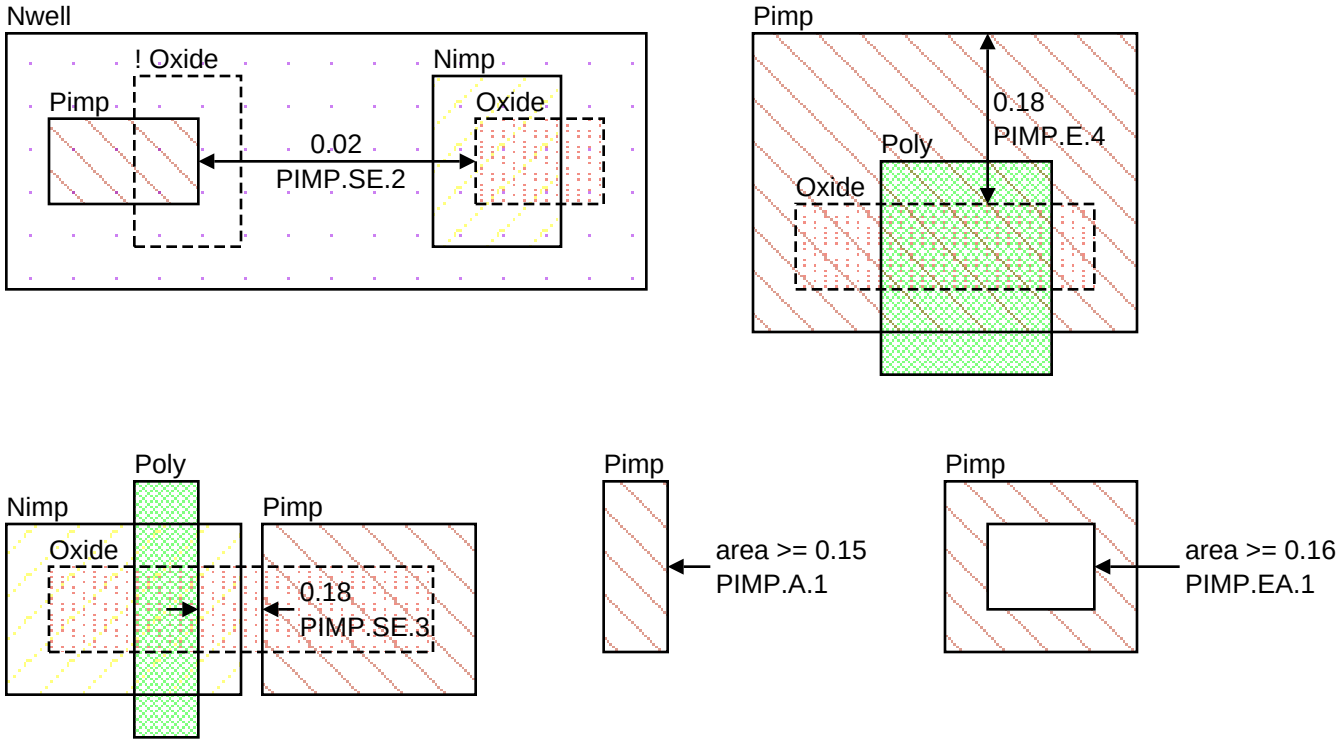
Rule Name	Value (um)	Description
PIMP.W.1	0.24	Minimum P+ Implant width.
PIMP.SP.1	0.24	Minimum P+ Implant space.
PIMP.E.1	0.14	Minimum P+ Implant to Active Area enclosure.
PIMP.O.1	0.16	Minimum P+ Implant to Active Area overlap.
PIMP.SE.1	0.16	Minimum P+ Implant to N+ Active (outside Nwell) Area spacing.
PIMP.E.2	0.02	Minimum P+ Implant to Active Area (substrate tie) enclosure.
PIMP.E.3	0.18	Minimum P+ Implant to gate side enclosure.
PIMP.SE.2	0.02	Minimum P+ Implant to N+ Active Area (Nwell tie) spacing.
PIMP.E.4	0.18	Minimum P+ to gate (endcap) enclosure.
PIMP.SE.3	0.18	Minimum P+ Implant to N+ gate side (butted Implant) spacing.
PIMP.A.1	0.15	Minimum area for P+ Implant.
PIMP.EA.1	0.16	Minimum P+ Implant ring enclosed area ("donut" hole surrounded by P+ Implant).
PIMP.X.1	---	P+ Implant is NOT allowed over N+ Implant.







P+ IMPLANT RULES (continued)

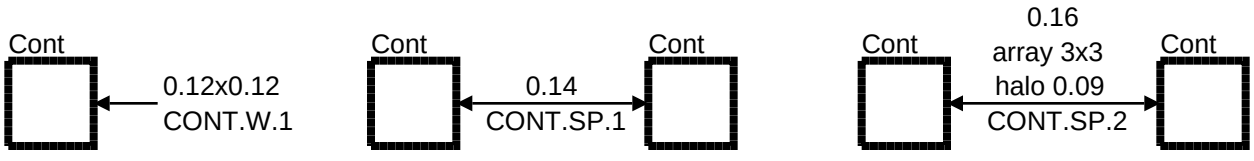


PIMP.X.1 - Covered by NIMP.X.1.

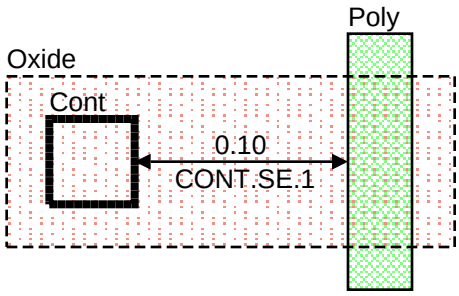
CONTACT RULES

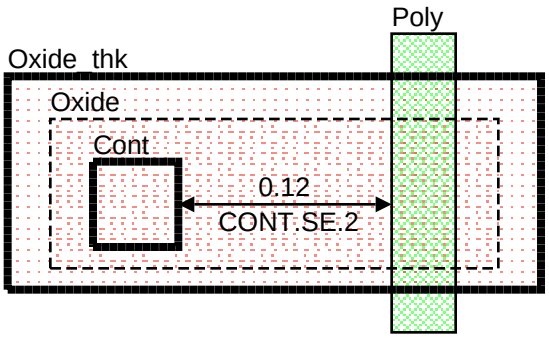
CONTACT RULES

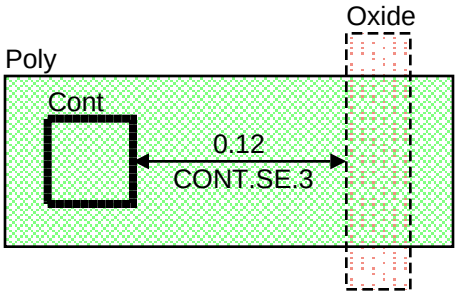
Rule Name	Value (um)	Description
CONT.W.1	0.12	Maximum and minimum Contact width/length.
CONT.SP.1	0.14	Minimum Contact to Contact spacing.
CONT.SP.2	0.16	Minimum Contact to Contact spacing when the Contacts are in a 3x3 or larger array (minimum dimension on one side of array is 3). Contacts spaced less than 0.18um should be considered for array spacing check.
CONT.SE.1	0.10	Minimum Contact on Active Area to gate spacing.
CONT.SE.2	0.12	Minimum Contact on 2.5V Active Area to gate spacing.
CONT.SE.3	0.12	Minimum gate Contact to Active Area spacing.
CONT.SE.4	0.14	Minimum 2.5V gate Contact to Active Area spacing.
CONT.SE.1.DFM	0.12	Minimum Contact on Active Area to gate spacing for DFM.
CONT.SE.2.DFM	0.14	Minimum Contact on 2.5V Active Area to gate spacing for DFM.
CONT.SE.3.DFM	0.14	Minimum gate Contact to Active Area spacing for DFM.
CONT.SE.4.DFM	0.16	Minimum 2.5V gate Contact to Active Area spacing for DFM.
CONT.E.1	0.06	Minimum Active Area to Contact enclosure.
CONT.E.2	0.04	Minimum Poly to Contact enclosure.
CONT.E.3	0.06	Minimum Poly to Contact enclosure on at least two opposite sides (end of line).
CONT.E.4	0.06	Minimum N+/P+ Implant on Active Area to Contact enclosure.
CONT.SE.5	0.24	Minimum Poly Contact to non-salacided Poly resistor or Active Contact to non-salacided Active resistor spacing.
CONT.X.1	---	Contact on gate is NOT allowed,
CONT.X.2	---	Active Area Contact on N+/P+ Implant edge is NOT allowed.
CONT.X.3	---	Contact must be covered by Metal1 and Active Area or Poly.

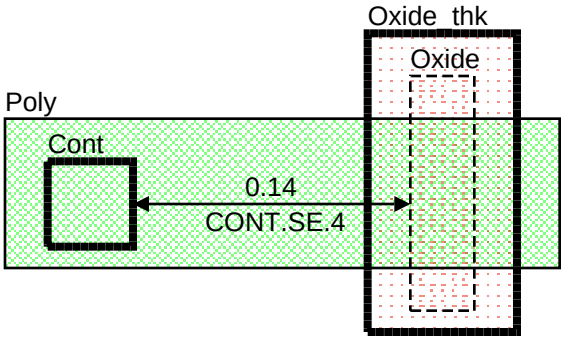


CONTACT RULES (continued)

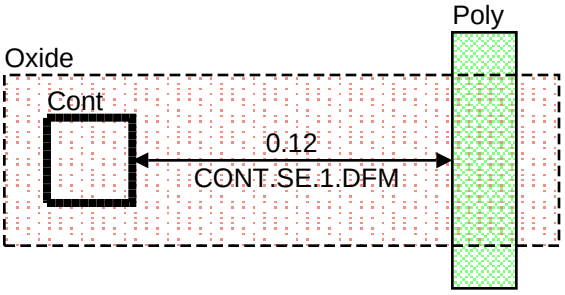


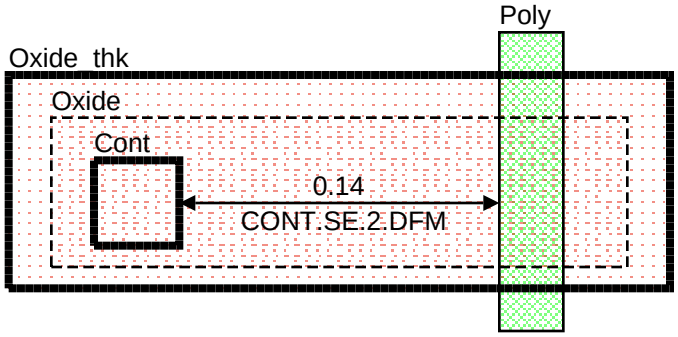


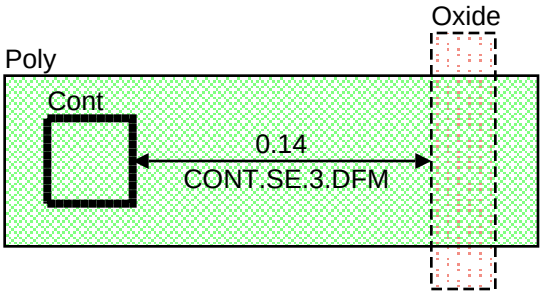


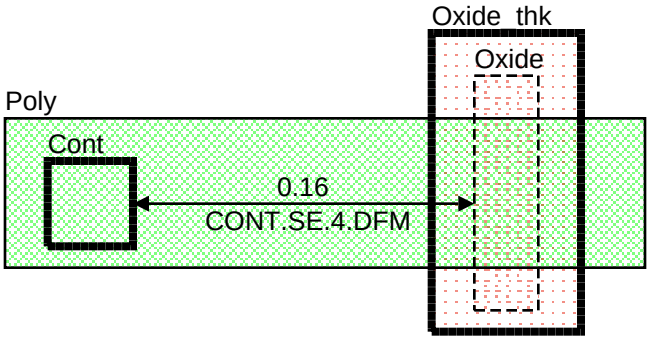


switch CHECK_DFM

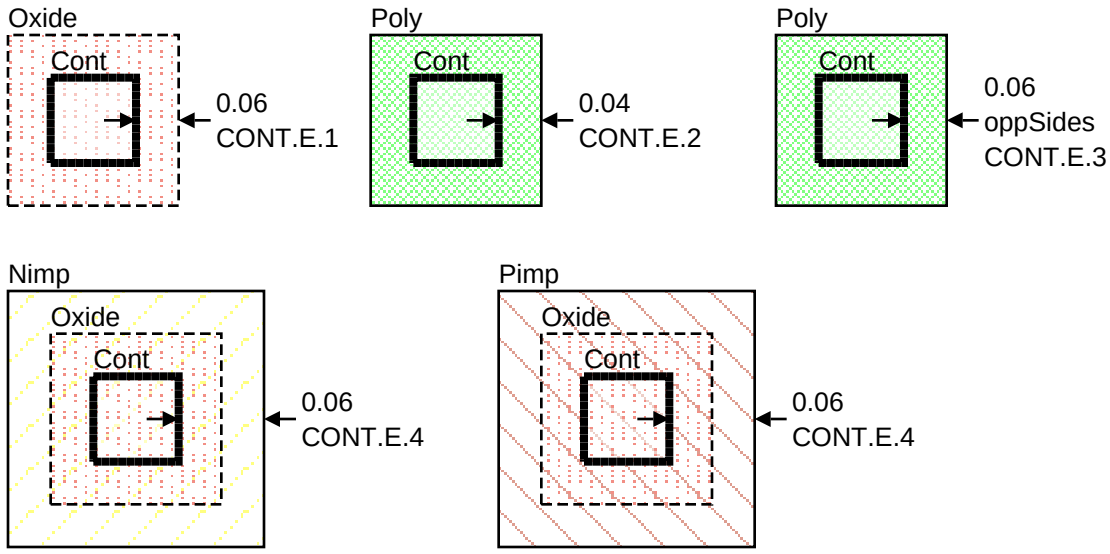




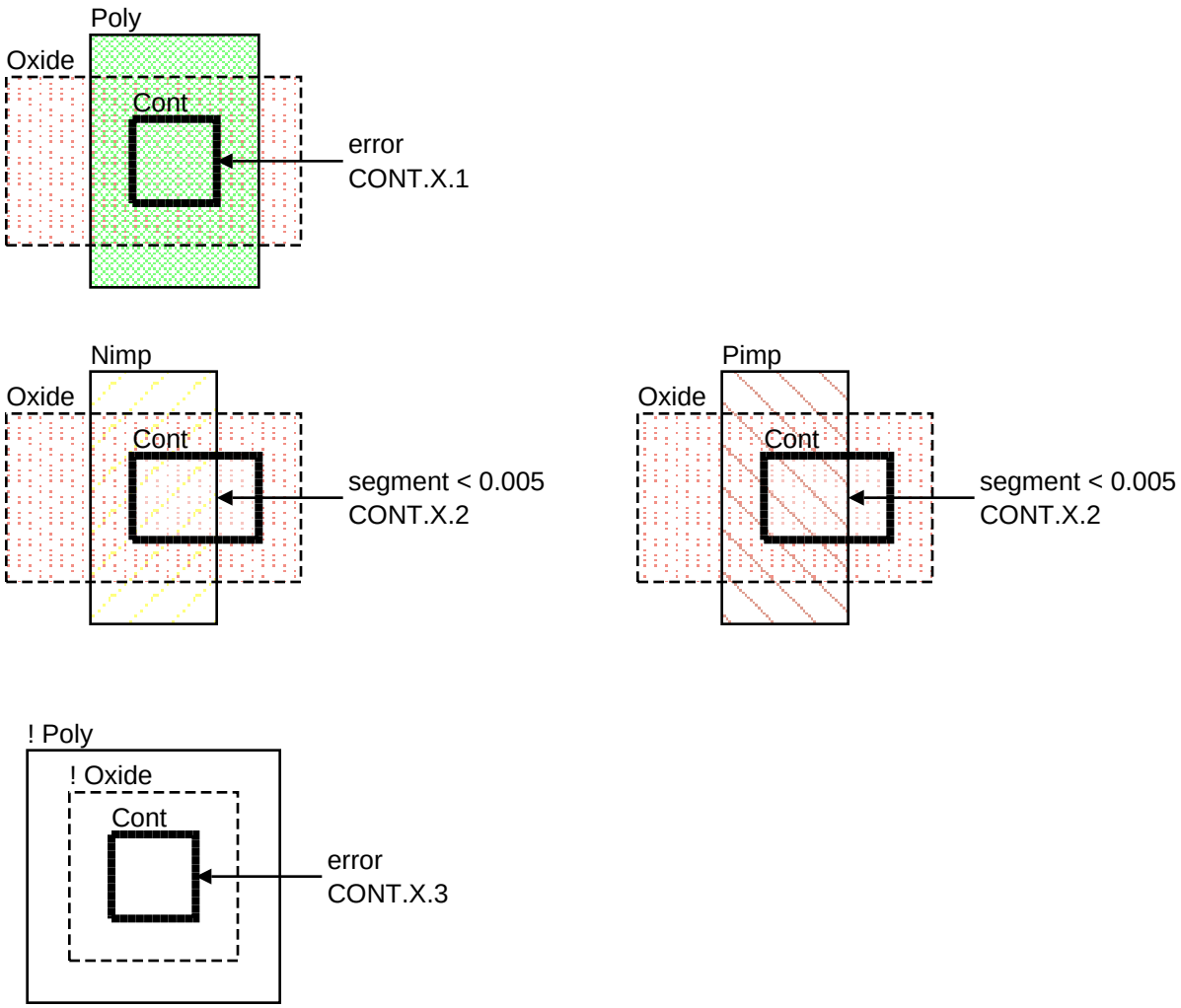




CONTACT RULES (continued)



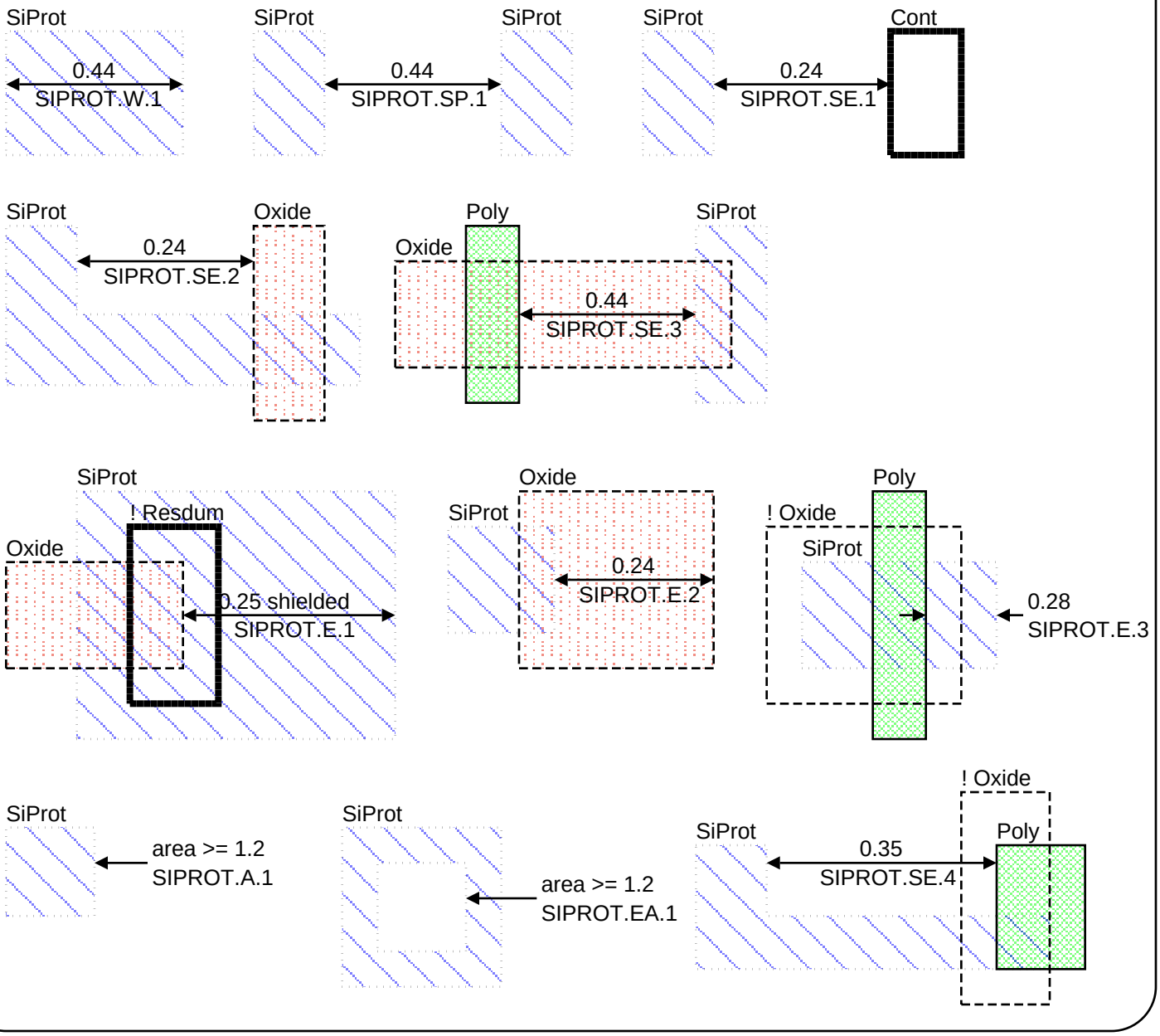
CONT.SE.5 - Covered by SIPROT.SE.1.



SALICIDE BLOCKING RULES

SALICIDE BLOCKING RULES

Rule Name	Value (um)	Description
SIPROT.W.1	0.44	Minimum Salicide Block width.
SIPROT.SP.1	0.44	Minimum Salicide Block space.
SIPROT.SE.1	0.24	Minimum Salicide Block to Contact spacing.
SIPROT.SE.2	0.24	Minimum Salicide Block to unrelated Active Area spacing.
SIPROT.SE.3	0.44	Minimum Salicide Block to gate spacing.
SIPROT.E.1	0.25	Minimum Salicide Block to Active Area enclosure.
SIPROT.E.2	0.24	Minimum Active Area to Salicide Block enclosure.
SIPROT.E.3	0.28	Minimum Salicide Block to Poly (on field) enclosure.
SIPROT.A.1	1.2	Minimum Salicide Block area.
SIPROT.EA.1	1.2	Minimum Salicide Block enclosed area ("donut" hole surrounded by Salicide Block).
SIPROT.SE.4	0.35	Minimum Salicide Block to Poly (on field) spacing.



METAL 1 RULES

METAL 1 RULES

Rule Name	Value (um)	Description
METAL1.W.1	0.12	Minimum Metal 1 width.
METAL1.W.2	12.0	Maximum Metal 1 width.
METAL1.SP.1.1	0.12	Minimum Metal 1 to Metal 1 spacing.
		Minimum Metal 1 to Metal 1 spacing if:
METAL1.SP.1.2	0.18	one metal width > 0.18 and parallel length > 0.56.
METAL1.SP.1.3	0.50	one metal width > 1.5 and parallel length > 1.5.
METAL1.SP.1.4	0.90	one metal width > 3.0 and parallel length > 3.0.
METAL1.SP.1.5	1.50	one metal width > 4.5 and parallel length > 4.5.
METAL1.SP.1.6	2.50	one metal width > 7.5 and parallel length > 7.5.
METAL1.E.1	0.00	Minimum Metal 1 to Contact enclosure.
METAL1.E.2	0.06	Minimum Metal 1 to Contact enclsoure on two opposite sides of the Contact.
METAL1.L.1	0.18	Minimum bent Metal 1 (45 degree angle) length.
METAL1.SP.2	0.16	Minimum bent Metal 1 (45 degree angle) space.
METAL1.W.3	0.14	Minimum bent Metal 1 (45 degree angle) width.
METAL1.A.1	0.07	Minimum Metal1 area.
METAL1.D.1	> 20% < 65%	Metal 1 Density range over any 120um x 120um area (checked by stepping in 60um increments).
METAL1.D.2	< 60%	Maximum Metal 1 density over any 600um x 600um area (checked by stepping in 300um increments).

METAL k (k = 2, 3, 4, 5, 6, 7) RULES

METAL k (k = 2, 3, 4, 5, 6, 7) RULES

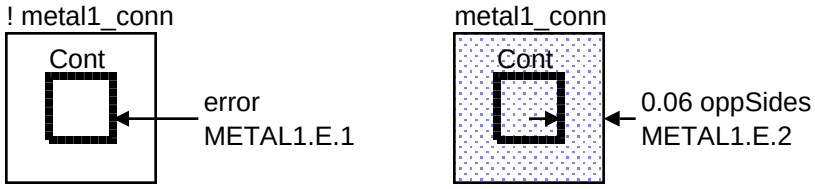
Rule Name	Value (um)	Description
METALk.W.1	0.14	Minimum Metal k width.
METALk.W.2	12.0	Maximum Metal k width.
METALk.SP.1.1	0.14	Minimum Metal k to Metal k spacing.
		Minimum Metal k to Metal k spacing if:
METALk.SP.1.2	0.20	one Metal k width > 0.20 and parallel length > 0.56.
METALk.SP.1.3	0.50	one Metal k width > 1.5 and parallel length > 1.5.
METALk.SP.1.4	0.90	one Metal k width > 3.0 and parallel length > 3.0.
METALk.SP.1.5	1.50	one Metal k width > 4.5 and parallel length > 4.5.
METALk.SP.1.6	2.50	one Metal k width > 7.5 and parallel length > 7.5.
METALk.E.1	0.005	Minimum Metal k enclosure of Via k-1.
METALk.E.2	0.06	Minimum Metal k enclosure of Via k-1on at least two opposite sides.
METALk.L.1	0.20	Minimum bent Metal k (45 degree angle) length.
METALk.SP.2	0.18	Minimum bent Metal k (45 degree angle) space.
METALk.W.3	0.16	Minimum bent Metal k (45 degree angle) width.
METALk.A.1	0.08	Minimum Metal k area.
METALk.D.1	> 20% < 65%	Metal k Density range over any 120um x 120um area (checked by stepping in 60um increments).
METALk.D.2	< 60%	Maximum Metal k density over any 600um x 600um area (checked by stepping in 300um increments).

METAL k (k = 8, 9) RULES

METAL k (k = 8, 9) RULES

Rule Name	Value (um)	Description
METALk.W.1	0.44	Minimum Metal k width.
METALk.W.2	12.0	Maximum Metal k width.
METALk.SP.1.1	0.40	Minimum Metal k to Metal k spacing.
		Minimum Metal k to Metal k spacing if:
METALk.SP.1.2	0.50	one Metal k width > 1.50 and parallel length > 1.50.
METALk.SP.1.3	0.90	one Metal k width > 3.00 and parallel length > 3.00.
METALk.SP.1.4	1.50	one Metal k width > 4.50 and parallel length > 4.50.
METALk.SP.1.5	2.50	one Metal k width > 7.5 and parallel length > 7.5.
METALk.E.1	0.05	Minimum Metal k overlap of Via k-1.
METALk.E.2	0.1	Minimum Metal k overlap of Via k-1 on at least two opposite sides.
METALk.A.1	0.20	Minimum Metal k area.
METALk.D.1	> 20% < 65%	Metal k Density range over any 120um x 120um area (checked by stepping in 60um increments).
METALk.D.2	< 60%	Maximum Metal k density over any 600um x 600um area (checked by stepping in 300um increments).

METAL RULES (continued)



macro

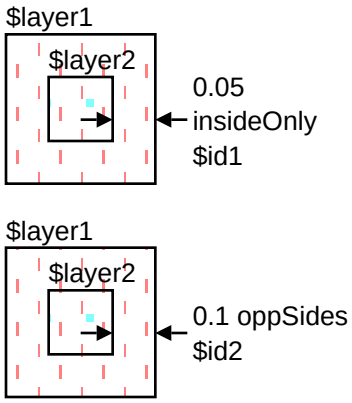
Macro Table

$name1	$layer1	$layer2	$id1	$id2
Metal2	metal2_conn	Via1	METAL2.E.1	METAL2.E.2
Metal3	metal3_conn	Via2	METAL3.E.1	METAL3.E.2
Metal4	metal4_conn	Via3	METAL4.E.1	METAL4.E.2
Metal5	metal5_conn	Via4	METAL5.E.1	METAL5.E.2
Metal6	metal6_conn	Via5	METAL6.E.1	METAL6.E.2
Metal7	metal7_conn	Via6	METAL7.E.1	METAL7.E.2

macro

Macro Table

$name1	$layer1	$layer2	$id1	$id2
Metal8	metal8_conn	Via7	METAL8.E.1	METAL8.E.2
Metal9	metal9_conn	Via8	METAL9.E.1	METAL9.E.2

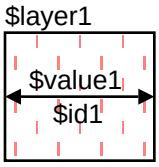


METAL RULES (continued)

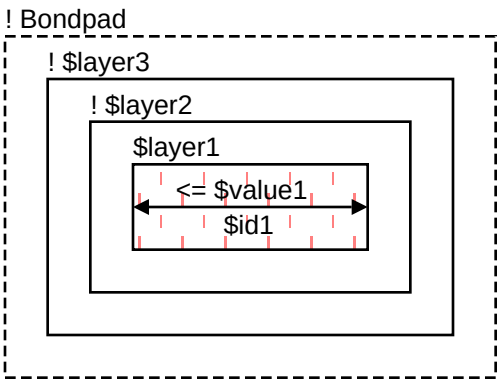
macro

Macro Table

$layer1	$name1	$id1	$value1
metal1_conn	Metal1	METAL1.W.1	0.12
metal2_conn	Metal2	METAL2.W.1	0.14
metal3_conn	Metal3	METAL3.W.1	0.14
metal4_conn	Metal4	METAL4.W.1	0.14
metal5_conn	Metal5	METAL5.W.1	0.14
metal6_conn	Metal6	METAL6.W.1	0.14
metal7_conn	Metal7	METAL7.W.1	0.14
metal8_conn	Metal8	METAL8.W.1	0.44
metal9_conn	Metal9	METAL9.W.1	0.44

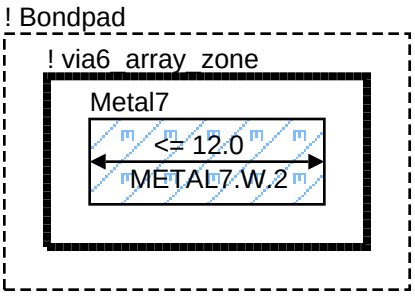


macro



Macro Table

$layer1	$layer2	$layer3	$name1	$id1	$value1
metal1_conn	cont_array_zone	via1_array_zone	Metal1	METAL1.W.2	12.0
metal2_conn	via1_array_zone	via2_array_zone	Metal2	METAL2.W.2	12.0
metal3_conn	via2_array_zone	via3_array_zone	Metal3	METAL3.W.2	12.0
metal4_conn	via3_array_zone	via4_array_zone	Metal4	METAL4.W.2	12.0
metal5_conn	via4_array_zone	via5_array_zone	Metal5	METAL5.W.2	12.0
metal6_conn	via5_array_zone	via6_array_zone	Metal6	METAL6.W.2	12.0

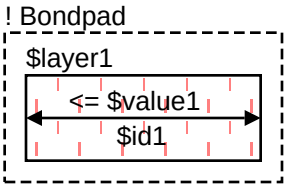


METAL RULES (continued)

macro

Macro Table

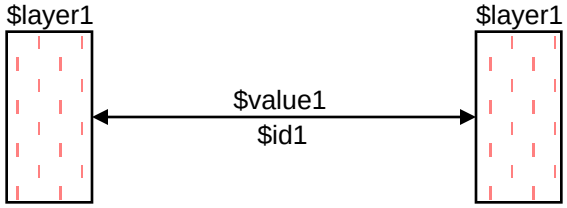
$layer1	$name1	$id1	$value1
metal8_conn	Metal8	METAL8.W.2	12.0
metal9_conn	Metal9	METAL9.W.2	12.0



macro

Macro Table

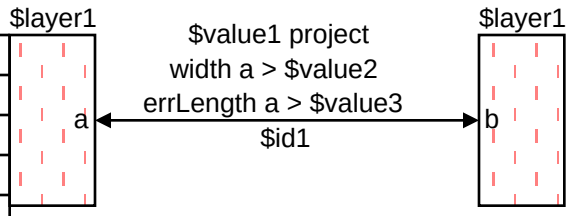
$layer1	$id1	$value1
Metal1	METAL1.SP.1.1	0.12
Metal2	METAL2.SP.1.1	0.14
Metal3	METAL3.SP.1.1	0.14
Metal4	METAL4.SP.1.1	0.14
Metal5	METAL5.SP.1.1	0.14
Metal6	METAL6.SP.1.1	0.14
Metal7	METAL7.SP.1.1	0.14
Metal8	METAL8.SP.1.1	0.40
Metal9	METAL9.SP.1.1	0.40



macro

Macro Table

$layer1	$id1	$value1	$value2	$value3
Metal1	METAL1.SP.1.2	0.18	0.18	0.56
Metal2	METAL2.SP.1.2	0.20	0.20	0.56
Metal3	METAL3.SP.1.2	0.20	0.20	0.56
Metal4	METAL4.SP.1.2	0.20	0.20	0.56
Metal5	METAL5.SP.1.2	0.20	0.20	0.56
Metal6	METAL6.SP.1.2	0.20	0.20	0.56
Metal7	METAL7.SP.1.2	0.20	0.20	0.56

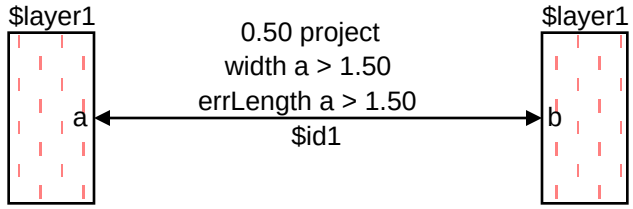


METAL RULES (continued)

macro

Macro Table

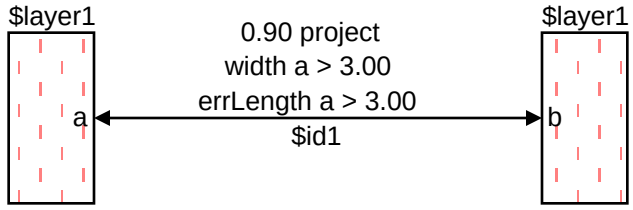
$layer1	$id1
Metal1	METAL1.SP.1.3
Metal2	METAL2.SP.1.3
Metal3	METAL3.SP.1.3
Metal4	METAL4.SP.1.3
Metal5	METAL5.SP.1.3
Metal6	METAL6.SP.1.3
Metal7	METAL7.SP.1.3
Metal8	METAL8.SP.1.2
Metal9	METAL9.SP.1.2



macro

Macro Table

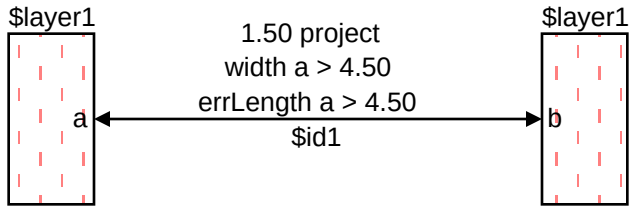
$layer1	$id1
Metal1	METAL1.SP.1.4
Metal2	METAL2.SP.1.4
Metal3	METAL3.SP.1.4
Metal4	METAL4.SP.1.4
Metal5	METAL5.SP.1.4
Metal6	METAL6.SP.1.4
Metal7	METAL7.SP.1.4
Metal8	METAL8.SP.1.3
Metal9	METAL9.SP.1.3



macro

Macro Table

$layer1	$id1
Metal1	METAL1.SP.1.5
Metal2	METAL2.SP.1.5
Metal3	METAL3.SP.1.5
Metal4	METAL4.SP.1.5
Metal5	METAL5.SP.1.5
Metal6	METAL6.SP.1.5
Metal7	METAL7.SP.1.5
Metal8	METAL8.SP.1.4
Metal9	METAL9.SP.1.4

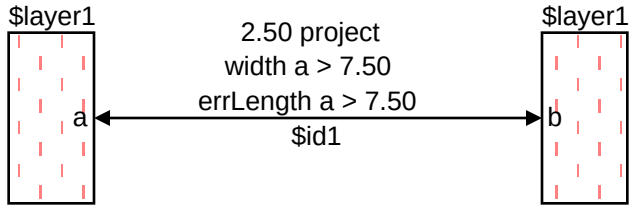


METAL RULES (continued)

macro

Macro Table

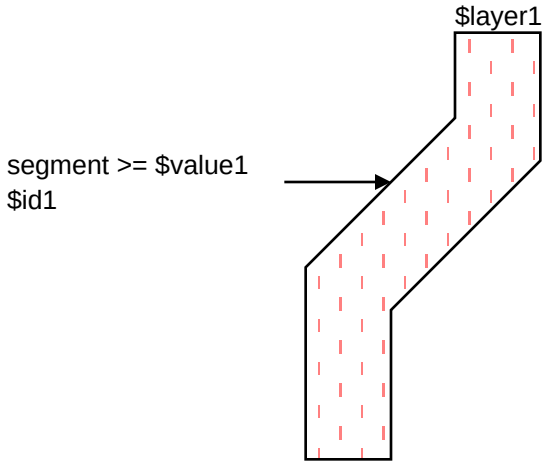
$layer1	$id1
Metal1	METAL1.SP.1.6
Metal2	METAL2.SP.1.6
Metal3	METAL3.SP.1.6
Metal4	METAL4.SP.1.6
Metal5	METAL5.SP.1.6
Metal6	METAL6.SP.1.6
Metal7	METAL7.SP.1.6
Metal8	METAL8.SP.1.5
Metal9	METAL9.SP.1.5



macro

Macro Table

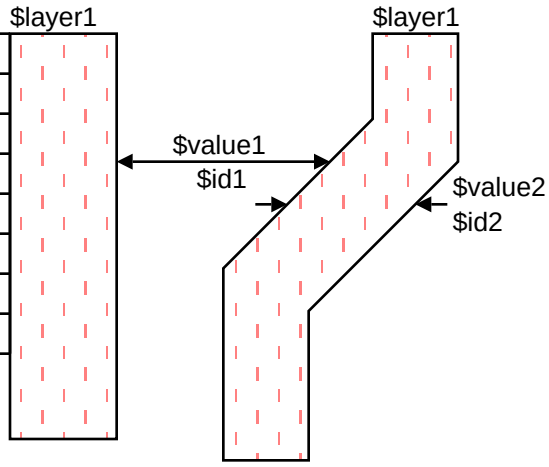
$layer1	$id1	$value1
Metal1	METAL1.L.1	0.18
Metal2	METAL2.L.1	0.20
Metal3	METAL3.L.1	0.20
Metal4	METAL4.L.1	0.20
Metal5	METAL5.L.1	0.20
Metal6	METAL6.L.1	0.20
Metal7	METAL7.L.1	0.20



macro

Macro Table

$layer1	$id1	$value1	$id2	$value2
Metal1	METAL1.SP.2	0.16	METAL1.W.3	0.14
Metal2	METAL2.SP.2	0.18	METAL2.W.3	0.16
Metal3	METAL3.SP.2	0.18	METAL3.W.3	0.16
Metal4	METAL4.SP.2	0.18	METAL4.W.3	0.16
Metal5	METAL5.SP.2	0.18	METAL5.W.3	0.16
Metal6	METAL6.SP.2	0.18	METAL6.W.3	0.16
Metal7	METAL7.SP.2	0.18	METAL7.W.3	0.16

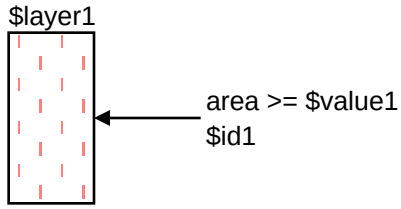


METAL RULES (continued)

macro

Macro Table

$layer1	$id1	$value1
Metal1	METAL1.A.1	0.07
Metal2	METAL2.A.1	0.08
Metal3	METAL3.A.1	0.08
Metal4	METAL4.A.1	0.08
Metal5	METAL5.A.1	0.08
Metal6	METAL6.A.1	0.08
Metal7	METAL7.A.1	0.08
Metal8	METAL8.A.1	0.2
Metal9	METAL9.A.1	0.2



METAL RULES (continued)

switch CHECK_DENSITY

macro

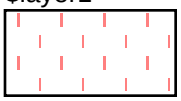
Macro Table

$name1	$layer1	$id1
Metal1	metal1_conn	METAL1.D.1
Metal2	metal2_conn	METAL2.D.1
Metal3	metal3_conn	METAL3.D.1
Metal4	metal4_conn	METAL4.D.1
Metal5	metal5_conn	METAL5.D.1
Metal6	metal6_conn	METAL6.D.1
Metal7	metal7_conn	METAL7.D.1
Metal8	metal8_conn	METAL8.D.1
Metal9	metal9_conn	METAL9.D.1

Density

ratio >= 0.20 <= 0.65
windowSize: 120.0
stepSize: 60.0
id: $id1
message: $name1 density must be >= 20% <= 65%

$layer1



macro

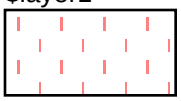
Macro Table

$name1	$layer1	$id1
Metal1	metal1_conn	METAL1.D.2
Metal2	metal2_conn	METAL2.D.2
Metal3	metal3_conn	METAL3.D.2
Metal4	metal4_conn	METAL4.D.2
Metal5	metal5_conn	METAL5.D.2
Metal6	metal6_conn	METAL6.D.2
Metal7	metal7_conn	METAL7.D.2
Metal8	metal8_conn	METAL8.D.2
Metal9	metal9_conn	METAL9.D.2

Density

ratio <= 0.60
windowSize: 600.0
stepSize: 300.0
id: $id1
message: $name1 density must be <= 60%

$layer1



VIA k (k = 1, 2, 3, 4, 5, 6) RULES

VIA k (k = 1, 2, 3, 4, 5, 6) RULES

Rule Name	Value (um)	Description
VIAk.W.1	0.14	Minimum and maximum Via k width.
VIAk.SP.1	0.15	Minimum Via k to Via k spacing.
VIAk.SP.2	0.20	Minimum Via k to Via k spacing when the Via ks are in a 3x3 or larger array (minimum dimension on one side of array is 3). Via ks spaced less than 0.21um should be considered for array spacing check.
VIAk.E.1	0.005	Minimum Metal k to Via k enclosure.
VIAk.E.2	0.06	Minimum Metal k to Via k enclosure on at least two opposite sides of Via k.
VIAk.X.1	---	Minimum of two Via k with spacing <= 0.30um or four Via k with spacing <= 0.60um are required when connecting Metal k and Metal k+1 when one of the Metals has a width > 0.40um at the connection point.
VIAk.X.2	---	Minimum of four Via k with spacing <= 0.30um or nine Via k with spacing <= 0.60um are required when connecting Metal k and Metal k+1 when one of the Metals has a width > 1.0um at the connection point.
VIAk.X.3	---	Vias 1 through 6 may be consecutively stacked up to four high when only one Via is connecting two Metal layers for any level of the stack.
VIAk.X.4	---	Vias 1 through 6 may be consecutively stacked up more than four high when at least two Vias are connecting two Metal layers for all levels of the stack.

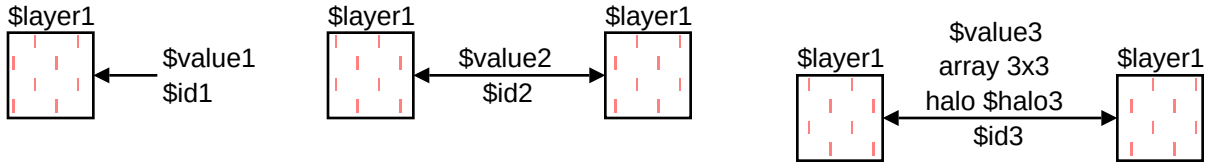
VIA 7, 8 RULES

VIA k (k = 7, 8) RULES

Rule Name	Value (um)	Description
VIAk.W.1	0.36	Minimum and maximum Via k width.
VIAk.SP.1	0.36	Minimum Via k space.
VIAk.E.1	0.03	Minimum Metal k to of Via k enclosure.
VIAk.E.2	0.08	Minimum Metal k to Via k enclosure on at least two opposite sides of Via k.

VIA RULES (continued)

macro



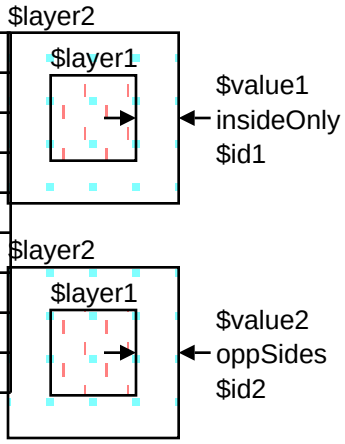
Macro Table

$layer1	$id1	$value1	$id2	$value2	$id3	$value3	$halo3
Via1	VIA1.W.1	0.14x0.14	VIA1.SP.1	0.15	VIA1.SP.2	0.20	0.10
Via2	VIA2.W.1	0.14x0.14	VIA2.SP.1	0.15	VIA2.SP.2	0.20	0.10
Via3	VIA3.W.1	0.14x0.14	VIA3.SP.1	0.15	VIA3.SP.2	0.20	0.10
Via4	VIA4.W.1	0.14x0.14	VIA4.SP.1	0.15	VIA4.SP.2	0.20	0.10
Via5	VIA5.W.1	0.14x0.14	VIA5.SP.1	0.15	VIA5.SP.2	0.20	0.10
Via6	VIA6.W.1	0.14x0.14	VIA6.SP.1	0.15	VIA6.SP.2	0.20	0.10
Via7	VIA7.W.1	0.36x0.36	VIA7.SP.1	0.36	ignore	ignore	ignore
Via8	VIA8.W.1	0.36x0.36	VIA8.SP.1	0.36	ignore	ignore	ignore

macro

Macro Table

$name1	$layer1	$layer2	$id1	$value1	$id2	$value2
Metal1	Via1	metal1_conn	VIA1.E.1	0.005	VIA1.E.2	0.06
Metal2	Via2	metal2_conn	VIA2.E.1	0.005	VIA2.E.2	0.06
Metal3	Via3	metal3_conn	VIA3.E.1	0.005	VIA3.E.2	0.06
Metal4	Via4	metal4_conn	VIA4.E.1	0.005	VIA4.E.2	0.06
Metal5	Via5	metal5_conn	VIA5.E.1	0.005	VIA5.E.2	0.06
Metal6	Via6	metal6_conn	VIA6.E.1	0.005	VIA6.E.2	0.06
Metal7	Via7	metal7_conn	VIA7.E.1	0.03	VIA7.E.2	0.08
Metal8	Via8	metal8_conn	VIA8.E.1	0.03	VIA8.E.2	0.08

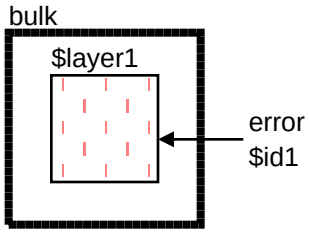


VIA RULES (continued)

macro

Macro Table

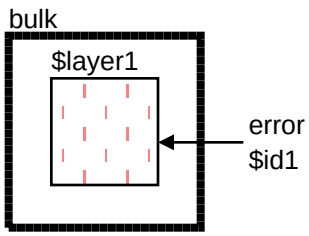
$name1	$name2	$name3	$layer1	$id1
Via1	Metal1	Metal2	rule_VIA1_X_1	VIA1.X.1
Via2	Metal2	Metal3	rule_VIA2_X_1	VIA2.X.1
Via3	Metal3	Metal4	rule_VIA3_X_1	VIA3.X.1
Via4	Metal4	Metal5	rule_VIA4_X_1	VIA4.X.1
Via5	Metal5	Metal6	rule_VIA5_X_1	VIA5.X.1
Via6	Metal6	Metal7	rule_VIA6_X_1	VIA6.X.1



macro

Macro Table

$name1	$name2	$name3	$layer1	$id1
Via1	Metal1	Metal2	rule_VIA1_X_2	VIA1.X.2
Via2	Metal2	Metal3	rule_VIA2_X_2	VIA2.X.2
Via3	Metal3	Metal4	rule_VIA3_X_2	VIA3.X.2
Via4	Metal4	Metal5	rule_VIA4_X_2	VIA4.X.2
Via5	Metal5	Metal6	rule_VIA5_X_2	VIA5.X.2
Via6	Metal6	Metal7	rule_VIA6_X_2	VIA6.X.2

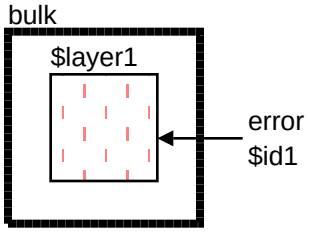


switch SUGGESTED_CHECK

macro

Macro Table

$name1	$name2	$layer1	$id1
Metal1	Metal6	rule_VIAk_X_3_X_4a	VIAk.X.3_VIAk.X.4
Metal2	Metal7	rule_VIAk_X_3_X_4b	VIAk.X.3_VIAk.X.4

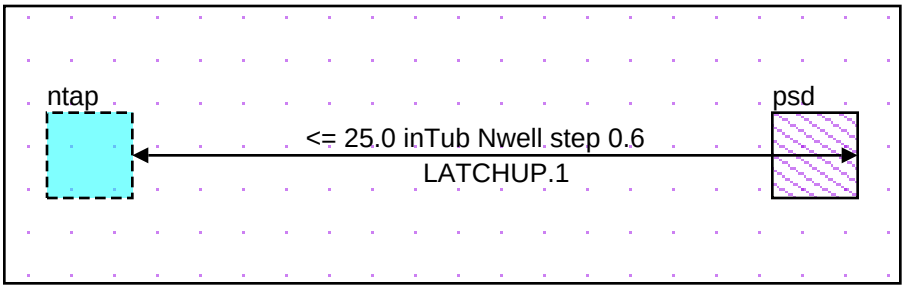


LATCH-UP RULES

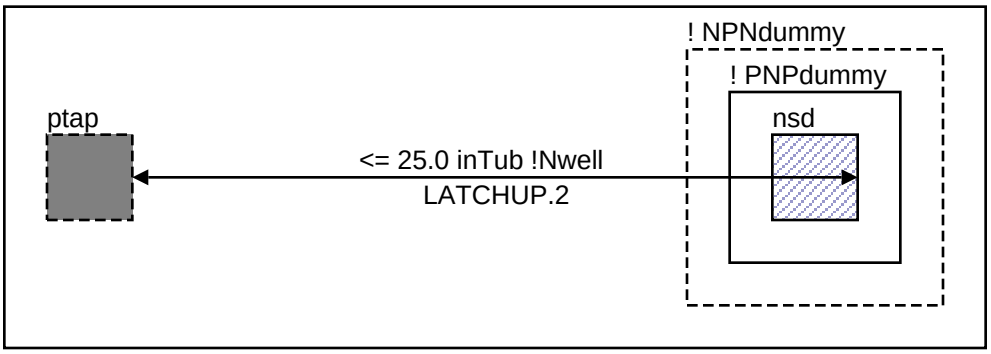
LATCH-UP RULES

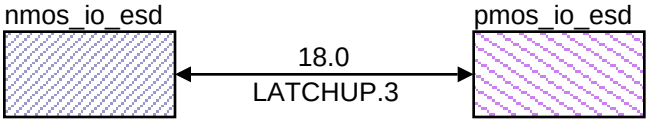
Rule Name	Value (um)	Description
LATCHUP.1	25.0	The maximum distance from any point in a P+ source/drain Active Area to the nearest Nwell pick-up in the same Nwell.
LATCHUP.2	25.0	The maximum distance from any point in an N+ source/drain Active Area to the nearest Psub pick-up in the same Psub.
LATCHUP.3	18.0	Minimum I/O or ESD NMOS to PMOS spacing.
LATCHUP.4	50.0	Minimum I/O or ESD NMOS to PMOS spacing when not blocked by a double guardring.

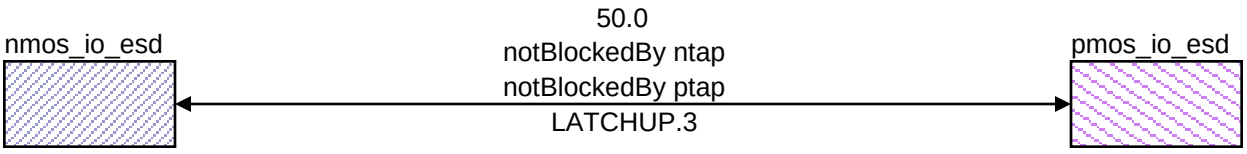
Nwell



! Nwell







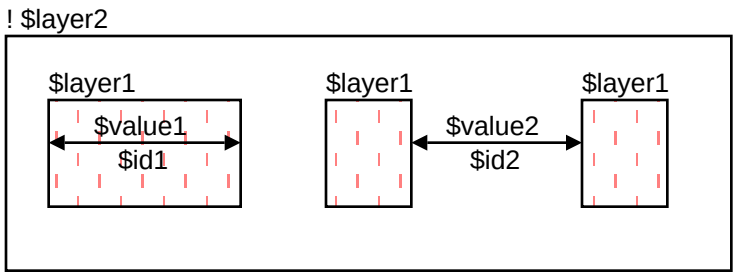
METAL k (k = 1, 2, 3, 4, 5, 6, 7, 8, 9) SLOT RULES

METAL k (k = 1, 2, 3, 4, 5, 6, 7, 8, 9) SLOT RULES

Rule Name	Value (um)	Description
MSLOTk.W.1	2.0	Minimum Metal k Slot width.
MSLOTk.L.1	2.0	Minimum Metal k Slot length.
MSLOTk.SP.1	M1/M2-7/M8,M9 0.12/0.14/0.44	Minimum Metal k Slot to Metal k Slot spacing (equal to the minimum Metal k width).
MSLOTk.E.1	M1/M2-7/M8,M9 0.12/0.14/0.44	Minimum Metal k to Metal k Slot enclosure (equal to the minimum Metal k width).
MSLOTk.X.1		Metal k Slots must be added to Metal k with both width and length greater than 12.0um.
MSLOTk.X.2		The length of Metal k Slots should be parallel to the direction of the current flow.
MSLOTk.X.3		Metal k Slot rules do not apply to Contact and Via array areas.
MSLOTk.X.4		Metal k Slot rules do not apply to bond pad areas.
MSLOTk.X.5		Metal k Slots must be rectangular or square.
MSLOTk.X.6		After Metal k Slots are added, Metal k must still meet density requirements.

Metal1-9 Slot Spacing Check & Width Check - with context

macro



Macro Table

$layer1	$layer2	$name1	$id1	$value1	$id2	$value2
Metal1_slot	Bondpad	Metal1 Slot	MSLOT1.W.1_MSLOT1.L.1	2.0	MSLOT1.SP.1	0.12
Metal2_slot	Bondpad	Metal2 Slot	MSLOT2.W.1_MSLOT2.L.1	2.0	MSLOT2.SP.1	0.14
Metal3_slot	Bondpad	Metal3 Slot	MSLOT3.W.1_MSLOT3.L.1	2.0	MSLOT3.SP.1	0.14
Metal4_slot	Bondpad	Metal4 Slot	MSLOT4.W.1_MSLOT4.L.1	2.0	MSLOT4.SP.1	0.14
Metal5_slot	Bondpad	Metal5 Slot	MSLOT5.W.1_MSLOT5.L.1	2.0	MSLOT5.SP.1	0.14
Metal6_slot	Bondpad	Metal6 Slot	MSLOT6.W.1_MSLOT6.L.1	2.0	MSLOT6.SP.1	0.14
Metal7_slot	Bondpad	Metal7 Slot	MSLOT7.W.1_MSLOT7.L.1	2.0	MSLOT7.SP.1	0.14
Metal8_slot	Bondpad	Metal8 Slot	MSLOT8.W.1_MSLOT8.L.1	2.0	MSLOT8.SP.1	0.44
Metal9_slot	Bondpad	Metal9 Slot	MSLOT9.W.1_MSLOT9.L.1	2.0	MSLOT9.SP.1	0.44

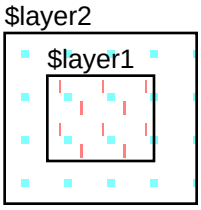
METAL k (k = 1, 2, 3, 4, 5, 6, 7, 8, 9) SLOT RULES (continued)

Metal1-9/Metal1-9 Slot Enclosure Check

macro

Macro Table

$layer1	$layer2	$name1	$id1	$value1
Metal1_slot_not_BP	Metal1	Metal1 Slot	MSLOT1.E.1	0.12
Metal2_slot_not_BP	Metal2	Metal2 Slot	MSLOT2.E.1	0.14
Metal3_slot_not_BP	Metal3	Metal3 Slot	MSLOT3.E.1	0.14
Metal4_slot_not_BP	Metal4	Metal4 Slot	MSLOT4.E.1	0.14
Metal5_slot_not_BP	Metal5	Metal5 Slot	MSLOT5.E.1	0.14
Metal6_slot_not_BP	Metal6	Metal6 Slot	MSLOT6.E.1	0.14
Metal7_slot_not_BP	Metal7	Metal7 Slot	MSLOT7.E.1	0.14
Metal8_slot_not_BP	Metal8	Metal8 Slot	MSLOT8.E.1	0.44
Metal9_slot_not_BP	Metal9	Metal9 Slot	MSLOT9.E.1	0.44



ANTENNA RULES

ANTENNA RULES

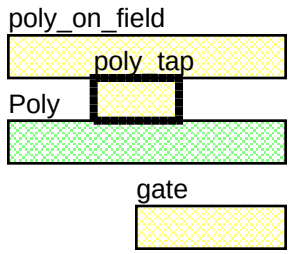
Rule Name	Value (um)	Description
ANT.1	275.0	Maximum ratio of Poly area to the gate area the Poly is connected to.
ANT.2	550.0	Maximum ratio of Poly sidewall area to the gate area the Poly is connected to.
ANT.3	15.0	Maximum ratio of Poly Contact area to the gate area the Contact is connected with.
ANT.4.Mx	475.0	Maximum ratio of single level Metal x (x = 1, 2, 3, 4, 5, 6, 7, 8, 9) area to the (gate area + 2*Diff area)
ANT.5.Vx	25.0	Maximum ratio of single level Via x (x = 1, 2, 3, 4, 5, 6, 7, 8) area to the (gate area + 2*Diff area)
ANT.6.Mx (x = 2, 3, 4, 5, 6, 7, 8, 9)	1200.0	Maximum ratio of cummulative multi level Metal areas to the (gate area + 2*Diff area)

Note 1: Source/drain diffusion areas of MOS devices are counted as part of the diode area.
Note 2: It is recommended to use one large diode with multiple Contacts rather than several smaller diodes.

ANTENNA RULES (continued)

switch !SKIP_CHECK_POLY_ANT_1

Antenna



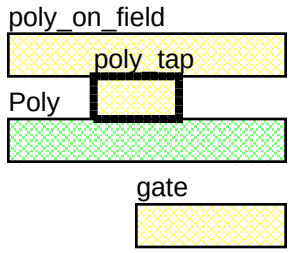
ratio (poly_on_field.area / gate.area) <= 275.0

id: ANT.1

message: Field Poly area to gate area ratio must be <= 275.0

switch !SKIP_CHECK_POLY_ANT_2

Antenna



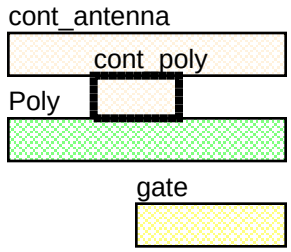
ratio (poly_on_field.perimeter / gate.area) <= 550.0

id: ANT.2

message: Field Poly perimeter to gate area ratio must be <= 550.0

switch !SKIP_CHECK_CONT_ANT_3

Antenna



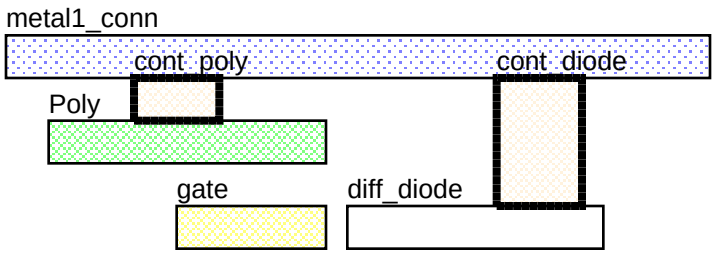
ratio (cont_antenna.area / gate.area) <= 15.0

id: ANT.3

message: Poly Contact area to gate area ratio must be <= 15.0

switch !SKIP_CHECK_METAL1_ANT_4

Antenna



ratio (metal1_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

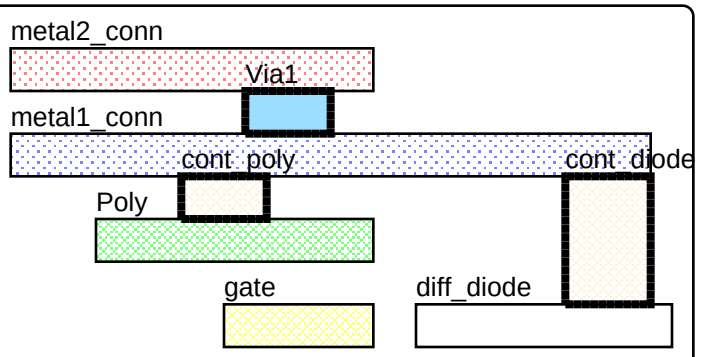
id: ANT.4.M1

message: Metal1 area / (gate area + 2*diff area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL2_ANT_4

Antenna



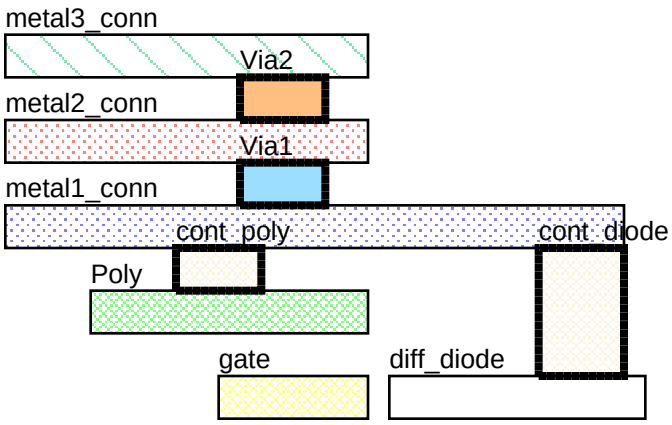
ratio (metal2_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

id: ANT.4.M2

message: Metal2 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

switch !SKIP_CHECK_METAL3_ANT_4

Antenna



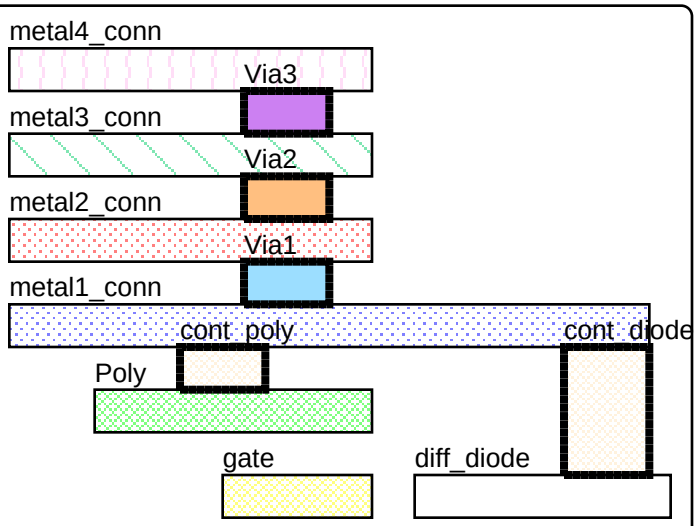
ratio (metal3_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

id: ANT.4.M3

message: Metal3 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

switch !SKIP_CHECK_METAL4_ANT_4

Antenna



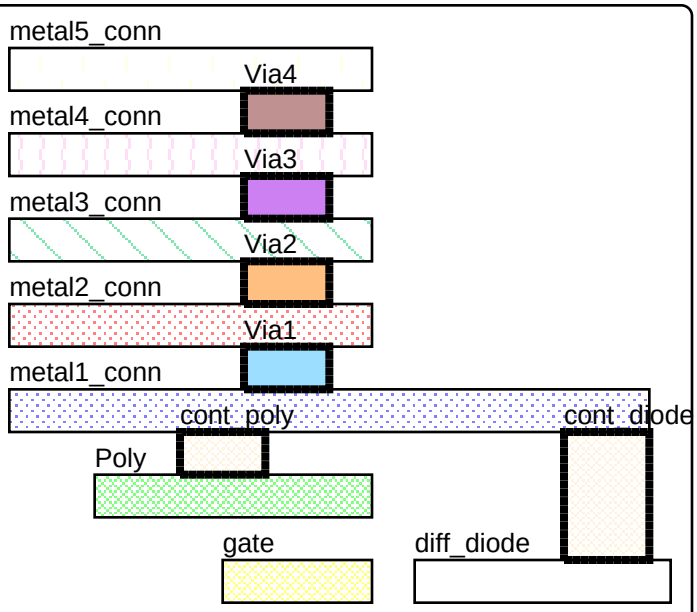
ratio (metal4_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

id: ANT.4.M4

message: Metal4 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

switch !SKIP_CHECK_METAL5_ANT_4

Antenna



ratio (metal5_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

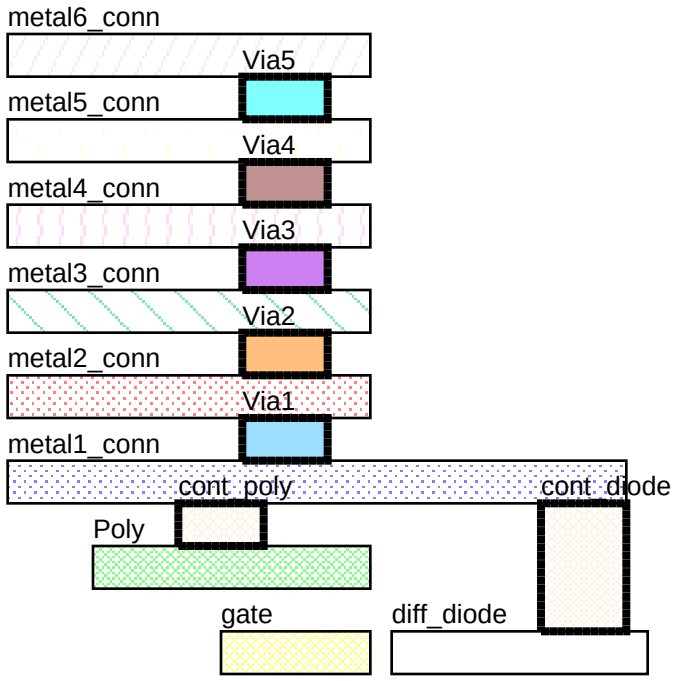
id: ANT.4.M5

message: Metal5 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL6_ANT_4

Antenna



ratio (metal6_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

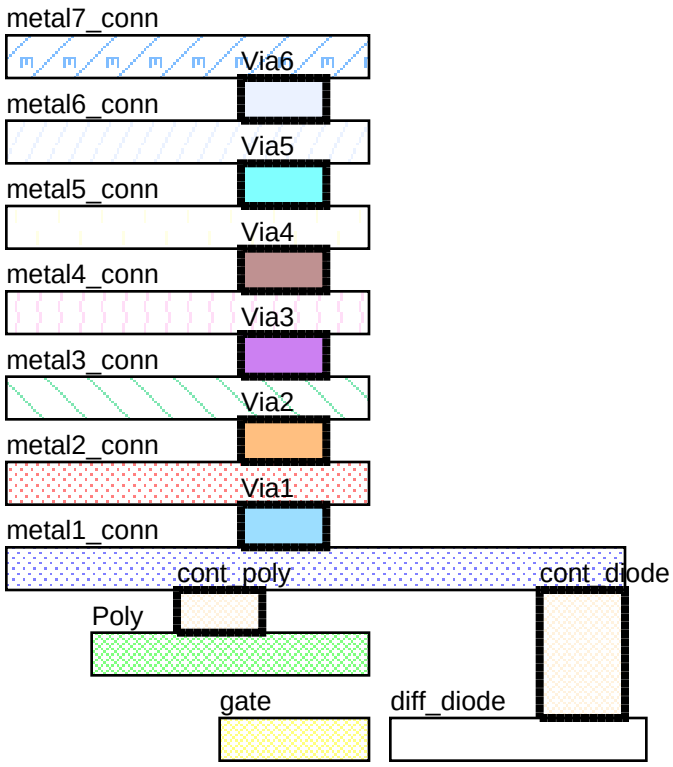
id: ANT.4.M6

message: Metal6 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL7_ANT_4

Antenna



ratio (metal7_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

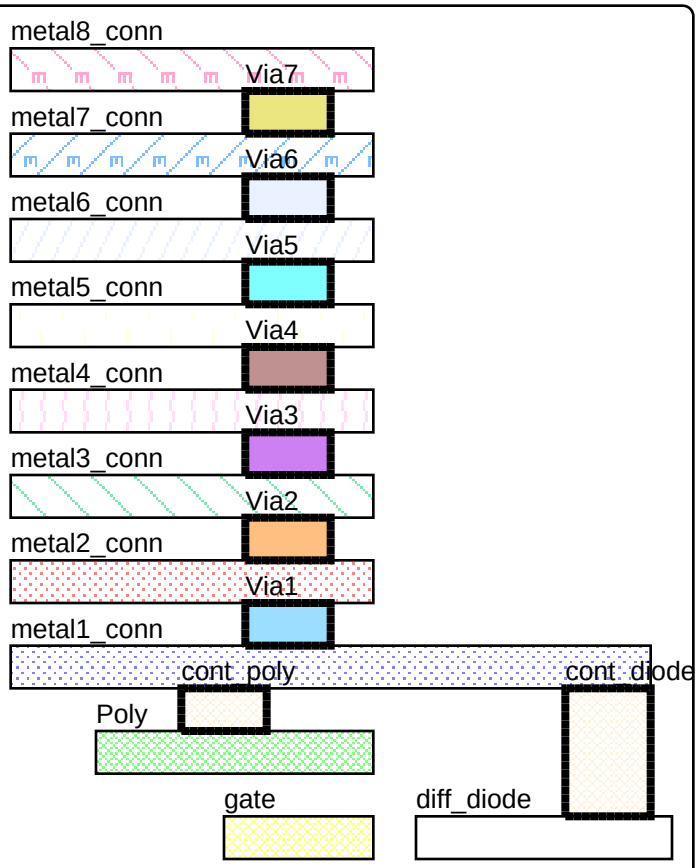
id: ANT.4.M7

message: Metal7 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL8_ANT_4

Antenna



ratio (metal8_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

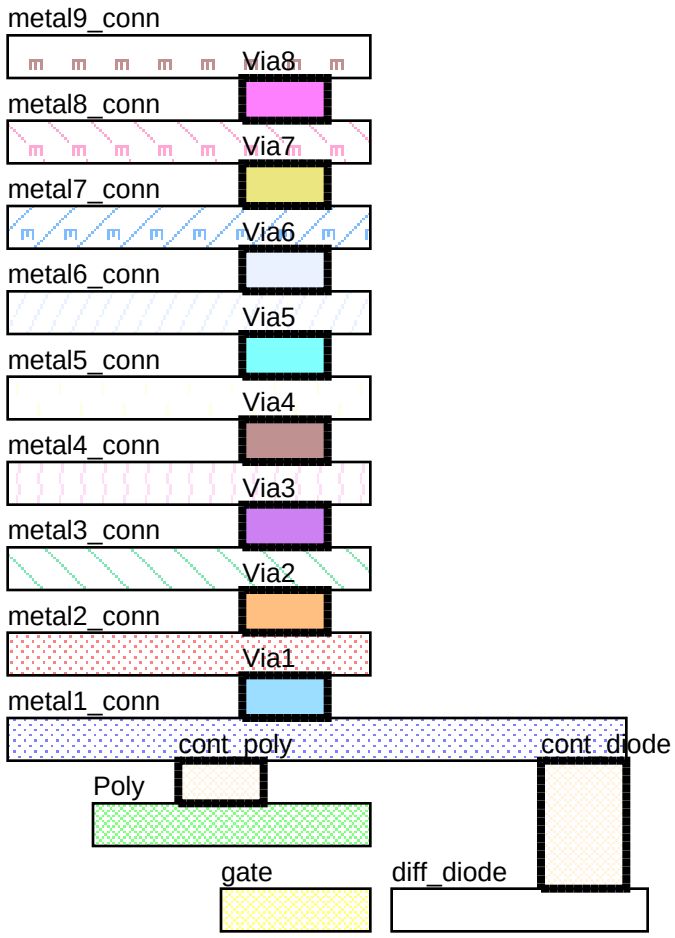
id: ANT.4.M8

message: Metal8 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL9_ANT_4

Antenna



ratio (metal9_conn.area / (gate.area + 2*diff_diode.area)) <= 475.0

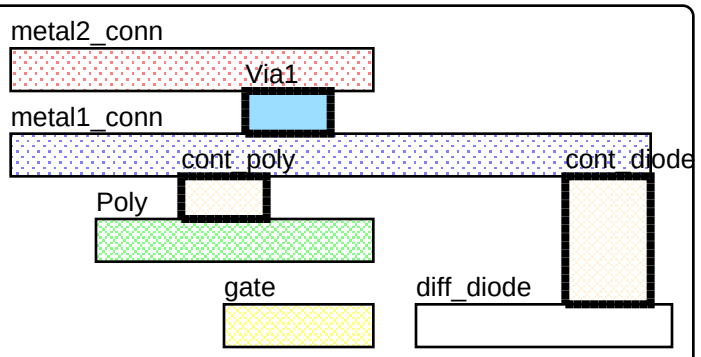
id: ANT.4.M9

message: Metal9 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA1_ANT_5

Antenna



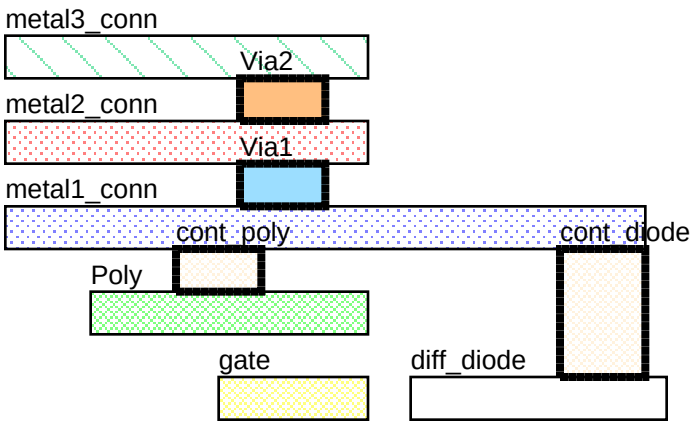
ratio (Via1.area / (gate.area + 2*diff_diode.area)) <= 25.0

id: ANT.5.V1

message: Via1 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

switch !SKIP_CHECK_VIA2_ANT_5

Antenna



ratio (Via2.area / (gate.area + 2*diff_diode.area)) <= 25.0

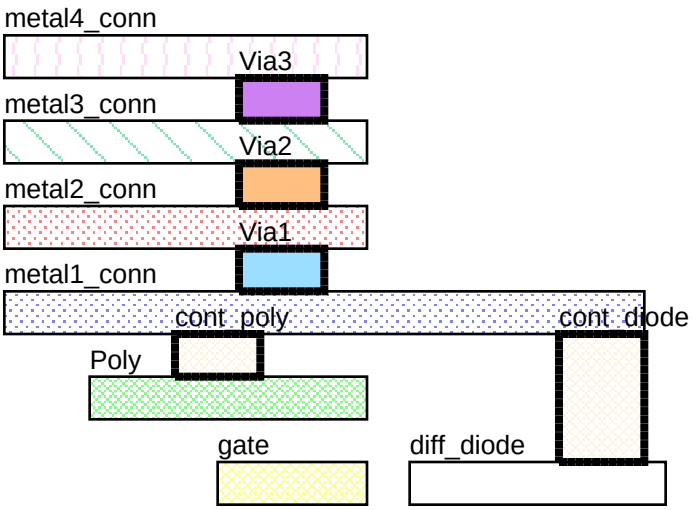
id: ANT.5.V2

message: Via2 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA3_ANT_5

Antenna



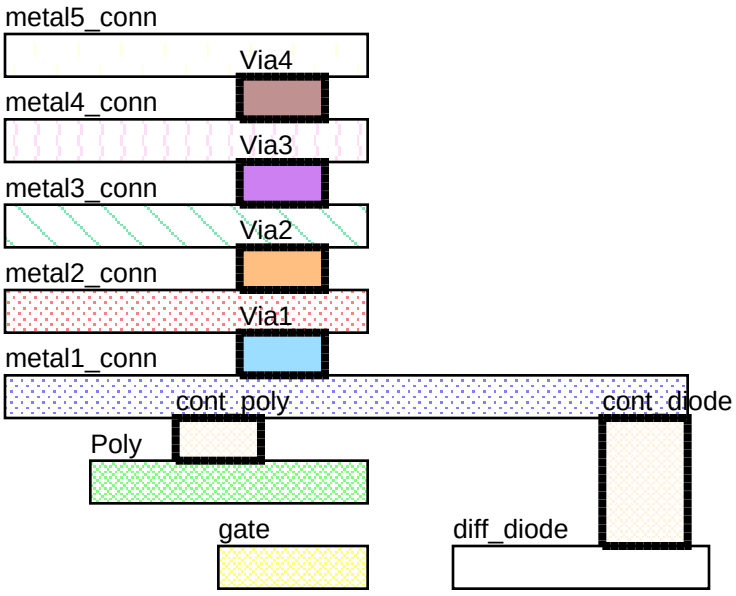
ratio (Via3.area / (gate.area + 2*diff_diode.area)) <= 25.0

id: ANT.5.V3

message: Via3 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

switch !SKIP_CHECK_VIA4_ANT_5

Antenna



ratio (Via4.area / (gate.area + 2*diff_diode.area)) <= 25.0

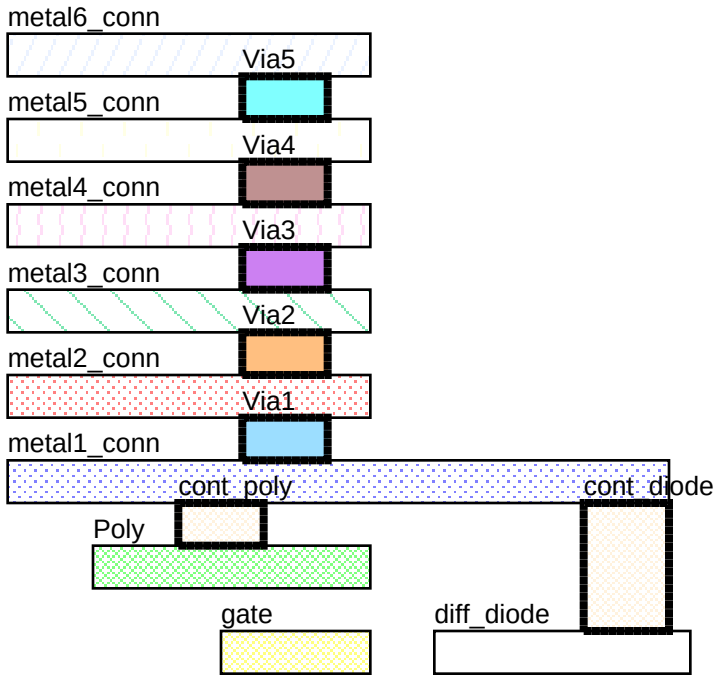
id: ANT.5.V4

message: Via4 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA5_ANT_5

Antenna



ratio (Via5.area / (gate.area + 2*diff_diode.area)) <= 25.0

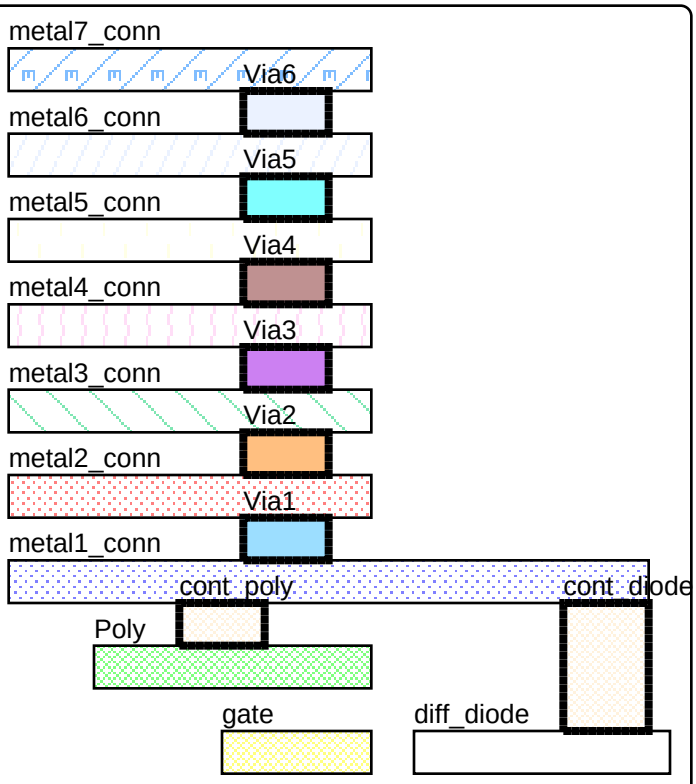
id: ANT.5.V5

message: Via5 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA6_ANT_5

Antenna



ratio (Via6.area / (gate.area + 2*diff_diode.area)) <= 25.0

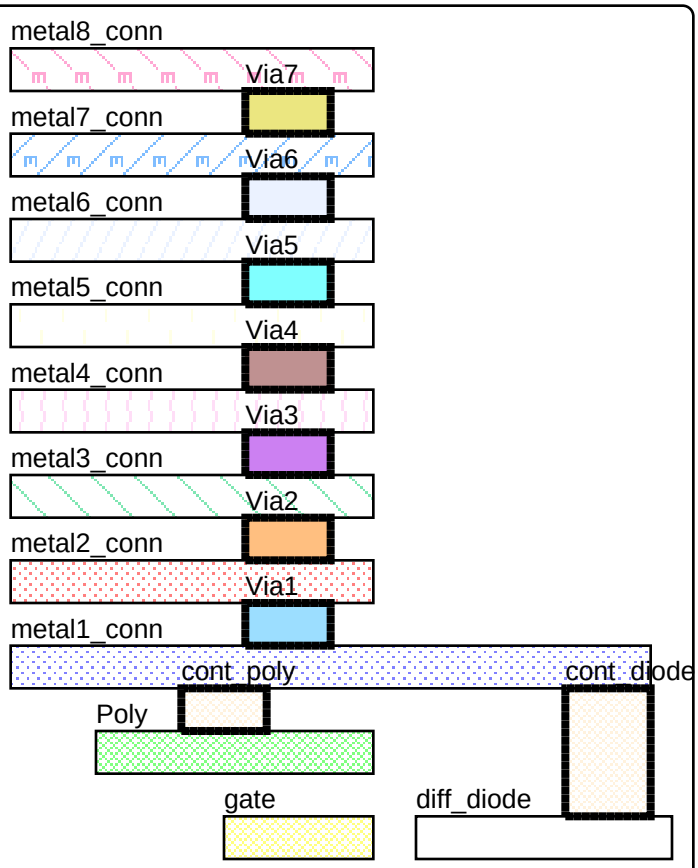
id: ANT.5.V6

message: Via6 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA7_ANT_5

Antenna



ratio (Via7.area / (gate.area + 2*diff_diode.area)) <= 25.0

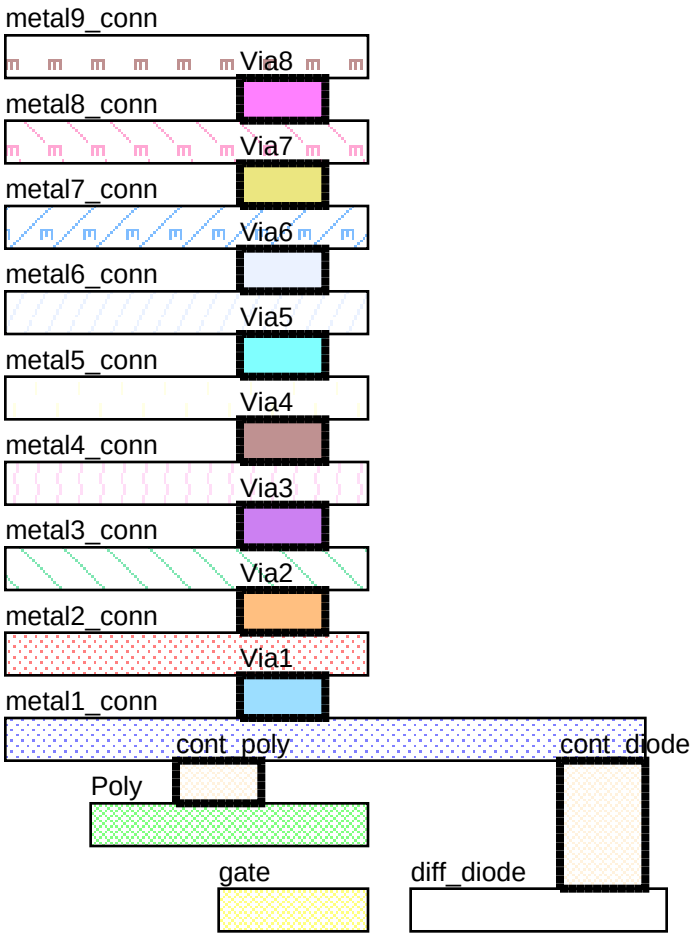
id: ANT.5.V7

message: Via7 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_VIA8_ANT_5

Antenna



ratio (Via8.area / (gate.area + 2*diff_diode.area)) <= 25.0

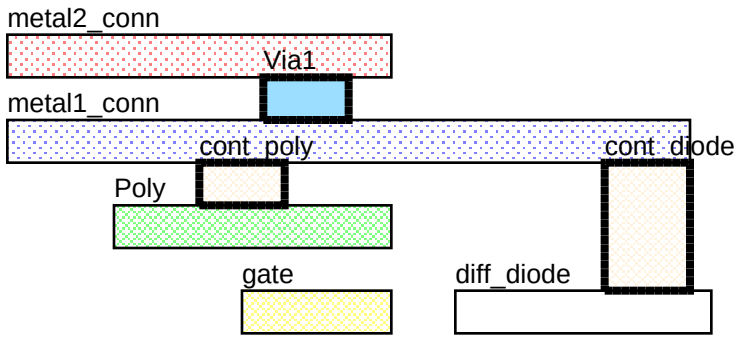
id: ANT.5.V8

message: Via8 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL2_ANT_6

Antenna



ratio ((metal2_conn.area + metal1_conn.area) /
(gate.area + 2*diff_diode.area)) <= 1200.0

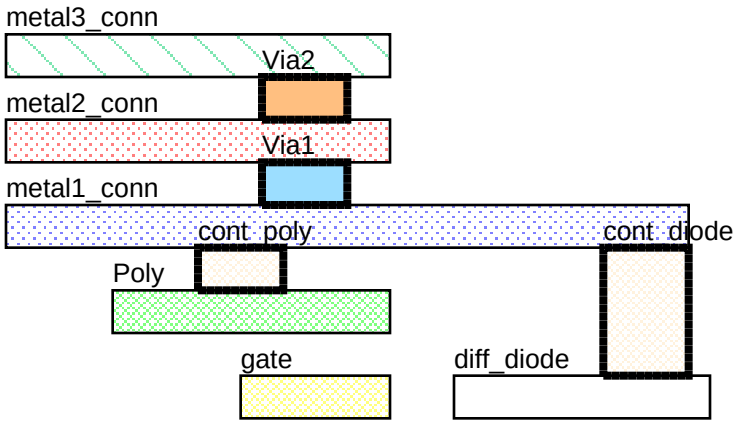
id: ANT.6.M2

message: Cumulative Metal1 through Metal2 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL3_ANT_6

Antenna



ratio ((metal3_conn.area + metal2_conn.area + metal1_conn.area) / (gate.area + 2*diff_diode.area)) <= 1200.0

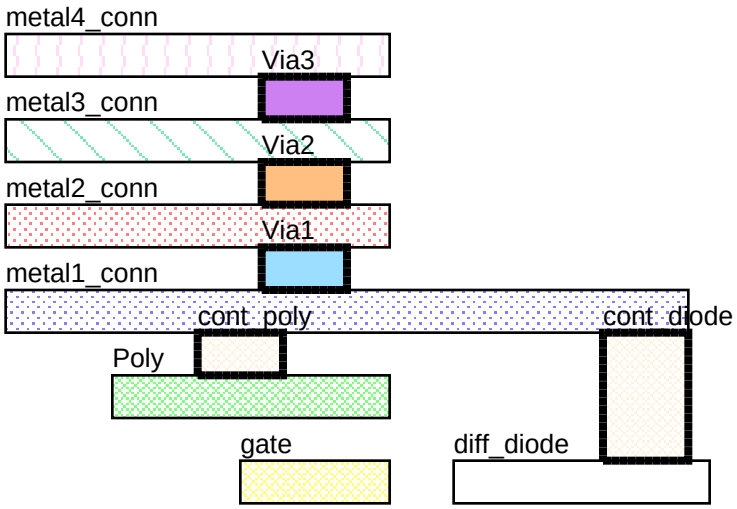
id: ANT.6.M3

message: Cumulative Metal1 through Metal3 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL4_ANT_6

Antenna



ratio ((metal4_conn.area +
metal3_conn.area + metal2_conn.area + metal1_conn.area) /
(gate.area + 2*diff_diode.area)) <= 1200.0

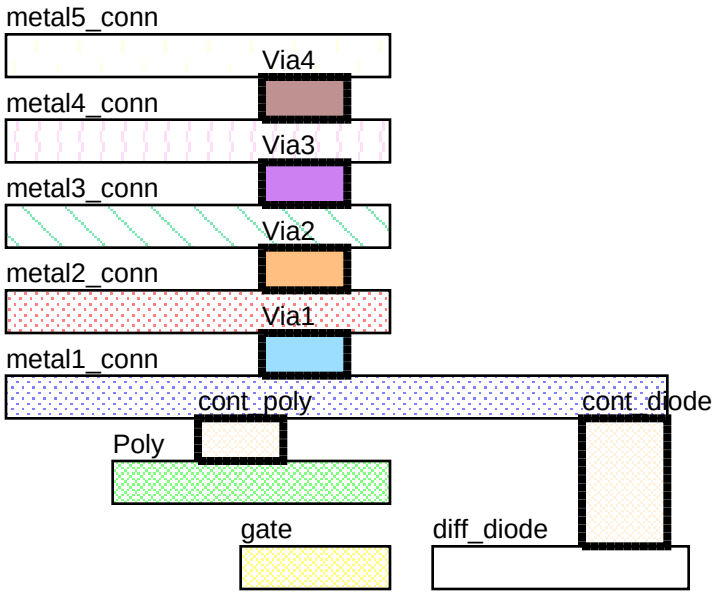
id: ANT.6.M4

message: Cumulative Metal1 through Metal4 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL5_ANT_6

Antenna



ratio ((metal5_conn.area + metal4_conn.area +
metal3_conn.area + metal2_conn.area + metal1_conn.area) /
(gate.area + 2*diff_diode.area)) <= 1200.0

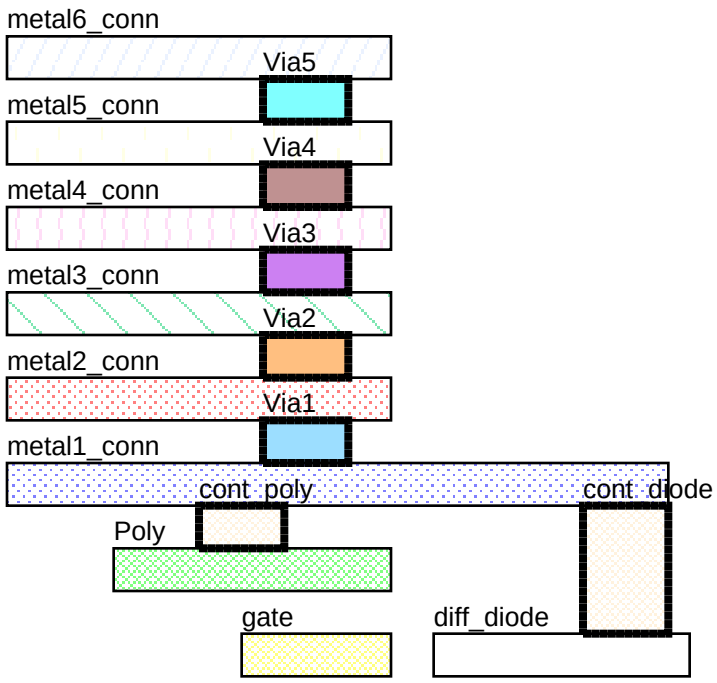
id: ANT.6.M5

message: Cumulative Metal1 through Metal5 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL6_ANT_6

Antenna



ratio ((metal6_conn.area + metal5_conn.area + metal4_conn.area + metal3_conn.area + metal2_conn.area + metal1_conn.area) / (gate.area + 2*diff_diode.area)) <= 1200.0

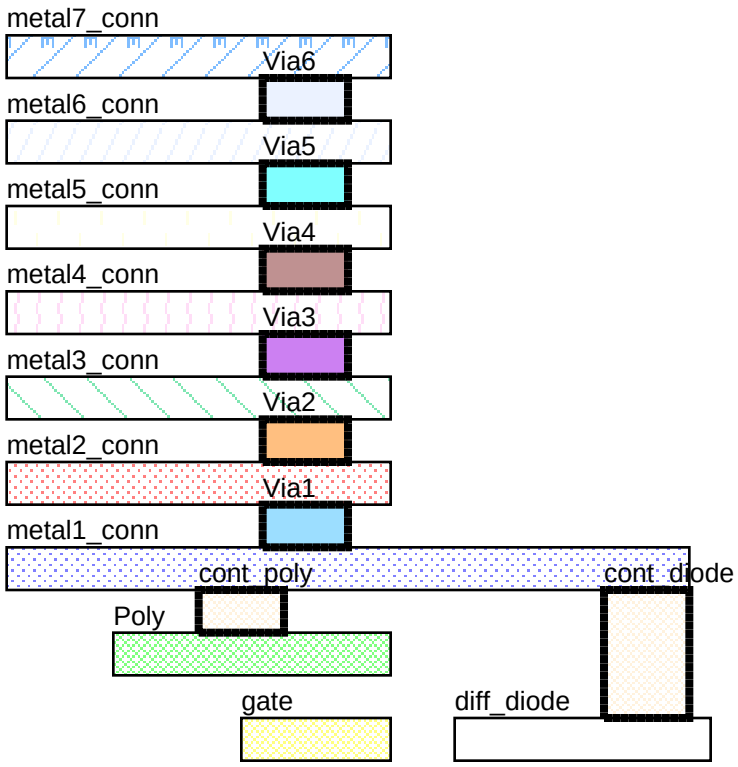
id: ANT.6.M6

message: Cumulative Metal1 through Metal6 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL7_ANT_6

Antenna



ratio ((metal7_conn.area +
metal6_conn.area + metal5_conn.area + metal4_conn.area +
metal3_conn.area + metal2_conn.area + metal1_conn.area) /
(gate.area + 2*diff_diode.area)) <= 1200.0

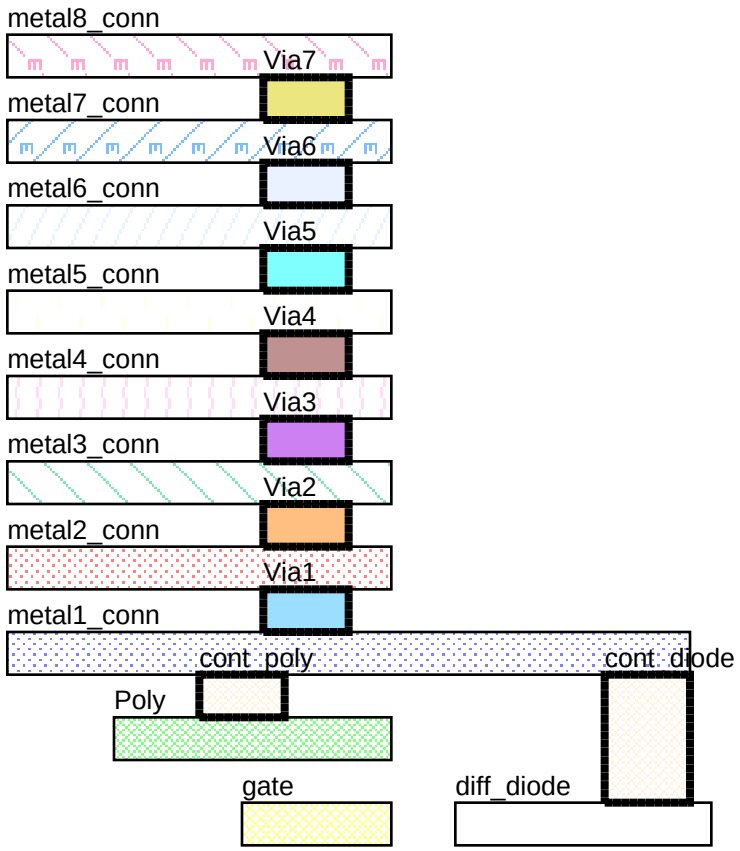
id: ANT.6.M7

message: Cumulative Metal1 through Metal7 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL8_ANT_6

Antenna



ratio ((metal8_conn.area + metal7_conn.area +
metal6_conn.area + metal5_conn.area + metal4_conn.area +
metal3_conn.area + metal2_conn.area + metal1_conn.area) /
(gate.area + 2*diff_diode.area)) <= 1200.0

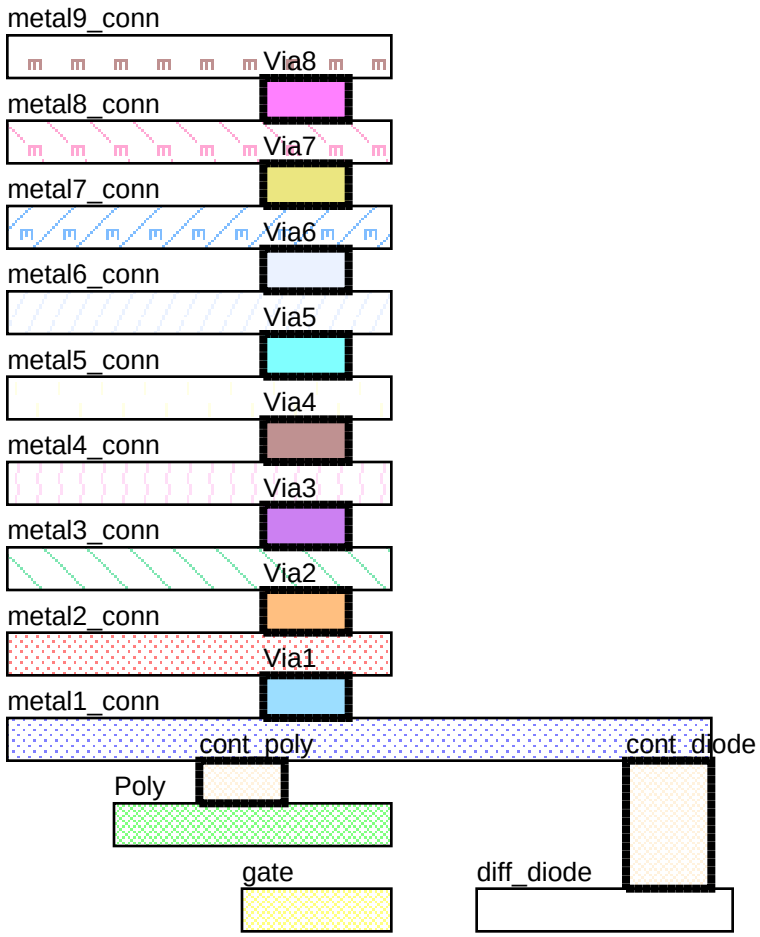
id: ANT.6.M8

message: Cumulative Metal1 through Metal8 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

ANTENNA RULES (continued)

switch !SKIP_CHECK_METAL9_ANT_6

Antenna



ratio ((metal9_conn.area + metal8_conn.area + metal7_conn.area + metal6_conn.area + metal5_conn.area + metal4_conn.area + metal3_conn.area + metal2_conn.area + metal1_conn.area) / (gate.area + 2*diff_diode.area)) <= 1200.0

id: ANT.6.M9

message: Cumulative Metal1 through Metal9 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0

CMOS I/O Design Rules

ESD Design Rules

The "ESDdummy" marker layer must be used to mark I/O ESD circuitry. If the "ESDdummy" layer is not used, the correct DRC checks of I/O ESD circuitry will not take place.

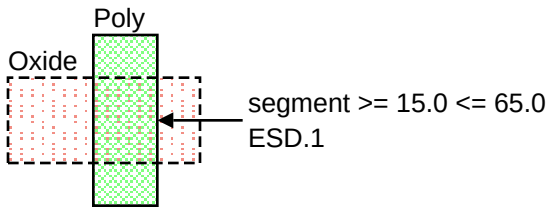
NMOS and PMOS devices used for ESD protection follow a strict finger structure using specific finger dimaensions and layout.

ESD Design Rules

Rule Name	Value (um)	Description
ESD.1	15 - 65	Width of each finger of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.
ESD.2	390	Minimum NMOS combined finger width for I/O buffers and for Vdd to Vss ESD protection.
ESD.3	390	Minimum PMOS combined finger width for I/O buffers.
ESD.4		Outer Oxide area of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection must be Source or connected to Bulk to prevent parasitic bipolars and unwanted discharge paths during ESD zapping.
ESD.5		NMOS ESD protection devices must be surrounded by a P+ Guard Ring.
ESD.6		PMOS ESD protection devices must be surrounded by an N+ Guard Ring.
ESD.7		NMOS and PMOS in ESD protection can NOT have butted taps.
ESD.8		NMOS and PMOS in an I/O buffer must have non-salicided Drains. The Contacts still must be salicided.
ESD.9		A P+ Oxide strap should be placed between N+ Oxides of different I/O and ESD devices when both connect to different pads.
ESD.10		An N+ Oxide strap should be placed between P+ Oxides of different I/O and ESD devices when both connect to different pads.
ESD.11	0.05	Minimum SiProt to Poly gate overlap in NMOS and PMOS drains.
ESD.12	1.8	Minimum enclosure of SiProt edge to Poly gate edge in NMOS and PMOS I/O drains.
ESD.13	1.8	Minimum SiProt to Oxide overlap in NMOS and PMOS I/O drains.
ESD.14	0.3	Exact gate length of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.
ESD.15	0.25	Minimum Poly gate to Contact spacing in NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.

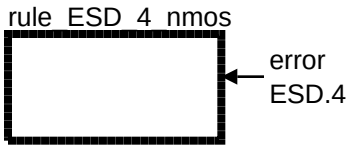
ESD Design Rules (continued)

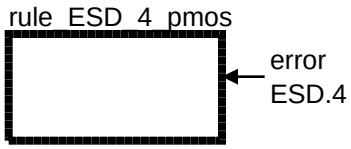
ESDdummy

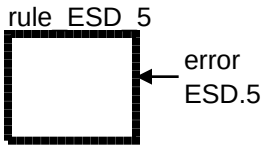


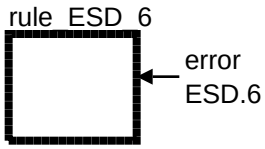
ESD.2 - Checked during LVS.

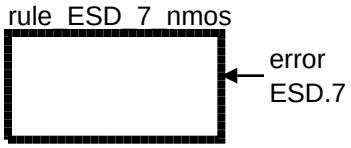
ESD.3 - Checked during LVS.

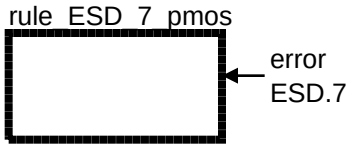


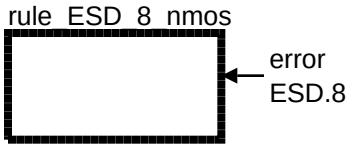


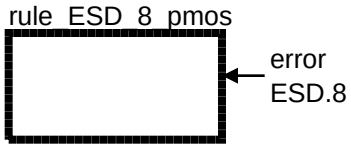


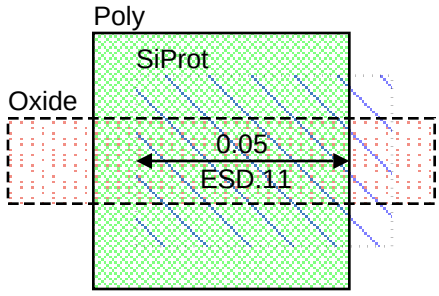


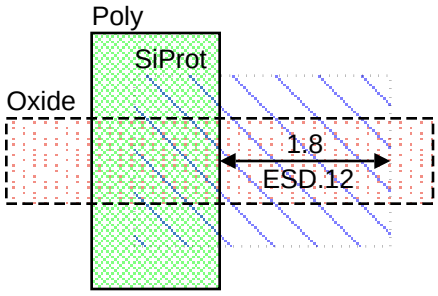






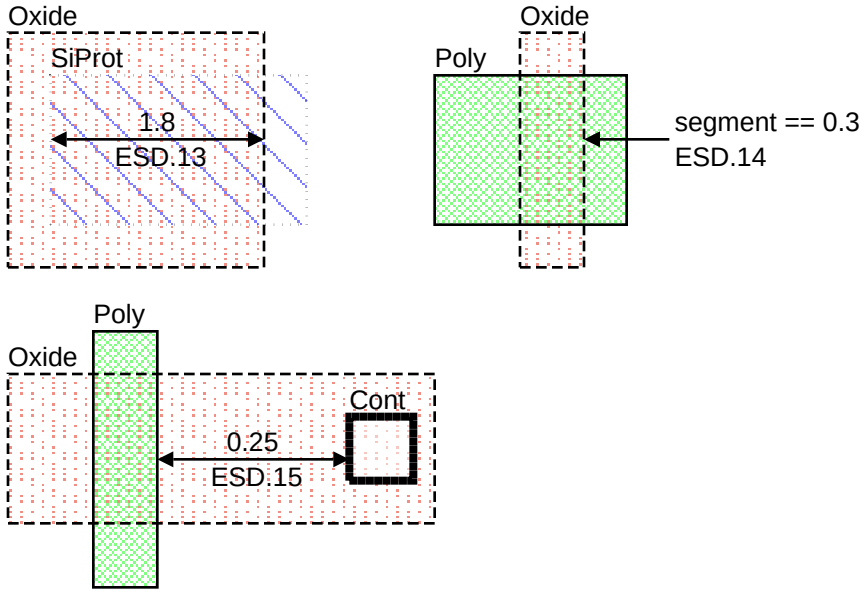






ESD Design Rules (continued)

ESDdummy



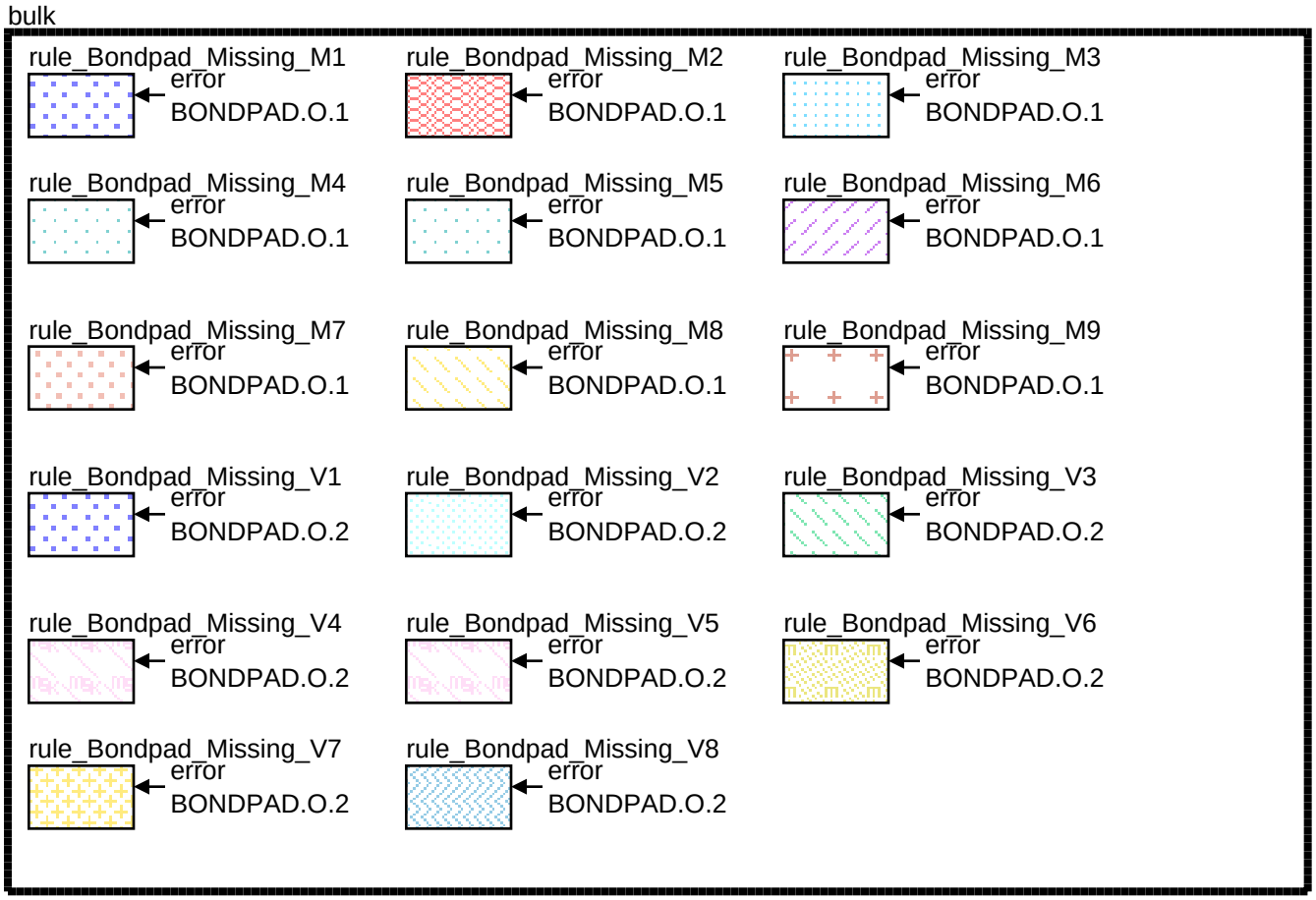
Bond Pad Design Rules

1) The bond pad structure must contain all Metal levels and all Via levels.
2) Metals over the Bonpad area are slotted with 1um slots spaced 1.5um.
3) The top metal is solid and does not contain stress slots.

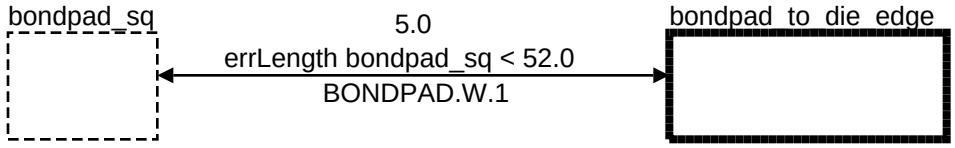
In-Line Bond Pad Design Rules

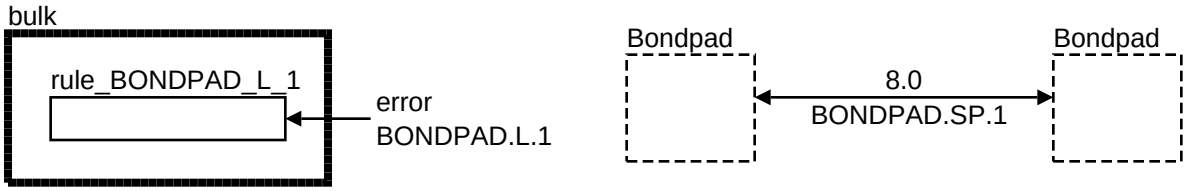
Rule Name	Value (um)	Description
BONDPAD.W.1	52.0	Minimum Bondpad width of edges parallel to the die edge.
BONDPAD.L.1	68.0	Minimum Bondpad length of edges perpendicular to the die edge.
BONDPAD.SP.1	8.0	Minimum Bondpad to Bondpad metal spacing.
BONDPAD.E.1	2.0	Minimum Metal (all levels) enclosure of Bondpad.
BONDPAD.SP.2	3.0	Minimum Bondpad Metal to Metal (including Bondpad Metal) spacing.
BONDPAD.B.1	1.8~3.2	Minimum length of Bonpad Metal beveled corner. All Bonpad Metal corners must be beveled at 45 degrees.
BONDPAD.W.2	0.14	Minimum and maximum Bondpad Via k width (k = 1, 2, 3, 4, 5, 6).
BONDPAD.W.3	0.36	Minimum and maximum Bondpad Via k width (k = 7, 8).
BONDPAD.SP.3	0.22	Minimum Bondpad Viak to Bondpad Viak spacing (k = 1, 2, 3, 4, 5, 6).
BONDPAD.SP.4	0.54	Minimum Bondpad Viak to Bondpad Viak spacing (k = 7, 8).
BONDPAD.E.2	0.05	Minimum Bondpad Metalk to Bondpad Viak enclosure (k = 1, 2, 3, 4, 5, 6). Minimum Bondpad Metalk+1 to Bondpad Viak enclosure (k = 1, 2, 3, 4, 5, 6).
BONDPAD.E.3	0.09	Minimum Bondpad Metalk to Bondpad Viak enclosure (k = 7, 8). Minimum Bondpad Metalk+1 to Bondpad Viak enclosure (k = 7, 8).
BONDPAD.R.1	16.0	Minimum Bondpad Viak inside Metalk to Metalk+1 crossing (k = 1, 2, 3, 4, 5, 6).
BONDPAD.R.2	4.0	Minimum Bondpad Viak inside Metalk to Metalk+1 crossing (k = 7, 8).
BONDPAD.SP.5	1.5	Minimum and Maximum Pad Metal slot to Pad Metal slot spacing.
BONDPAD.W.4	1.0	Minimum and Maximum Pad Metal slot width (expect first slot on each edge of Pad).
BONDPAD.W.5	5.0	Minimum and Maximum Pad Metalk width in outer ring of Pad Metalk (expect for the bevelled corners) (k = 1, 2, 3, 4, 5, 6, 7, 8).
BONDPAD.SP.6	1.0~3.5	Minimum and Maximum Pad Metalk ring to nearest Pad Metalk across first slot (k = 1, 2, 3, 4, 5, 6, 7, 8).
BONDPAD.SP.7	1.1	Minimum Pad Viak array to Pad Viak array spacing (k = 1, 2, 3, 4, 5, 6, 7, 8).

Bond Pad Design Rules (continued)



Bond Pad Design Rules (continued)

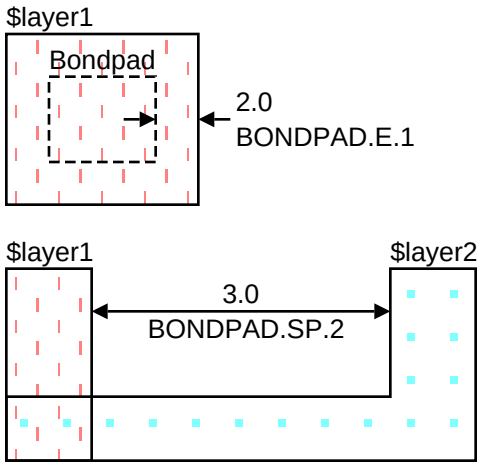




macro

Macro Table

$layer1	**$layer2**
bondpad_metal1_filled	Metal1
bondpad_metal2_filled	Metal2
bondpad_metal3_filled	Metal3
bondpad_metal4_filled	Metal4
bondpad_metal5_filled	Metal5
bondpad_metal6_filled	Metal6
bondpad_metal7_filled	Metal7
bondpad_metal8_filled	Metal8
bondpad_metal9_filled	Metal9

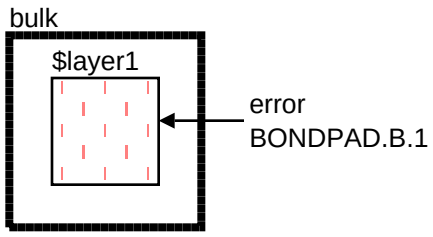


Bond Pad Design Rules (continued)

macro

Macro Table

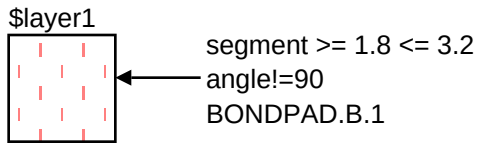
$layer1	$name1
rule_BONDPAD_B_1_m1	Metal1
rule_BONDPAD_B_1_m2	Metal2
rule_BONDPAD_B_1_m3	Metal3
rule_BONDPAD_B_1_m4	Metal4
rule_BONDPAD_B_1_m5	Metal5
rule_BONDPAD_B_1_m6	Metal6
rule_BONDPAD_B_1_m7	Metal7
rule_BONDPAD_B_1_m8	Metal8
rule_BONDPAD_B_1_m9	Metal9



macro

Macro Table

$layer1	$name1
bondpad_metal1_filled	Metal1
bondpad_metal2_filled	Metal2
bondpad_metal3_filled	Metal3
bondpad_metal4_filled	Metal4
bondpad_metal5_filled	Metal5
bondpad_metal6_filled	Metal6
bondpad_metal7_filled	Metal7
bondpad_metal8_filled	Metal8
bondpad_metal9_filled	Metal9



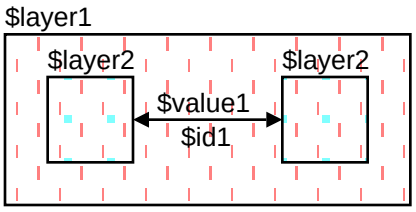
Bond Pad Design Rules (continued)

BONDPAD.W.2 and BONDPAD.W.3 - covered by VIAk.W.1.

macro

Macro Table

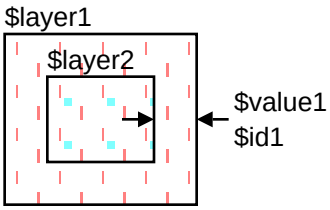
$layer1	$layer2	$value1	$id1
bondpad_metal1	Via1	0.22	BONDPAD.SP.3
bondpad_metal2	Via2	0.22	BONDPAD.SP.3
bondpad_metal3	Via3	0.22	BONDPAD.SP.3
bondpad_metal4	Via4	0.22	BONDPAD.SP.3
bondpad_metal5	Via5	0.22	BONDPAD.SP.3
bondpad_metal6	Via6	0.22	BONDPAD.SP.3
bondpad_metal7	Via7	0.54	BONDPAD.SP.4
bondpad_metal8	Via8	0.54	BONDPAD.SP.4



macro

Macro Table

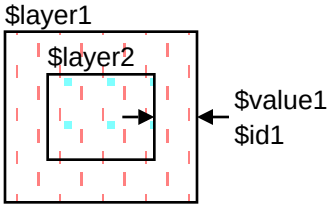
$layer1	$layer2	$name1	$value1	$id1
bondpad_metal1	Via1	Metal1	0.05	BONDPAD.E.2
bondpad_metal2	Via2	Metal2	0.05	BONDPAD.E.2
bondpad_metal3	Via3	Metal3	0.05	BONDPAD.E.2
bondpad_metal4	Via4	Metal4	0.05	BONDPAD.E.2
bondpad_metal5	Via5	Metal5	0.05	BONDPAD.E.2
bondpad_metal6	Via6	Metal6	0.05	BONDPAD.E.2
bondpad_metal7	Via7	Metal7	0.09	BONDPAD.E.3
bondpad_metal8	Via8	Metal8	0.09	BONDPAD.E.3



macro

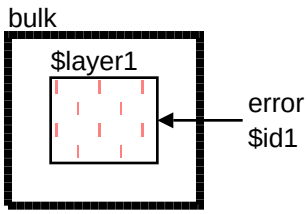
Macro Table

$layer1	$layer2	$name1	$value1	$id1
bondpad_metal2	Via1	Metal2	0.05	BONDPAD.E.2
bondpad_metal3	Via2	Metal3	0.05	BONDPAD.E.2
bondpad_metal4	Via3	Metal4	0.05	BONDPAD.E.2
bondpad_metal5	Via4	Metal5	0.05	BONDPAD.E.2
bondpad_metal6	Via5	Metal6	0.05	BONDPAD.E.2
bondpad_metal7	Via6	Metal7	0.05	BONDPAD.E.2
bondpad_metal8	Via7	Metal8	0.09	BONDPAD.E.3
bondpad_metal9	Via8	Metal9	0.09	BONDPAD.E.3



Bond Pad Design Rules (continued)

macro



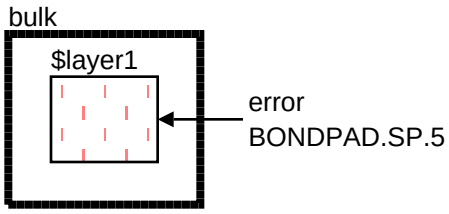
Macro Table

$layer1	$name1	$name2	$name3	$value	$id1
rule_BONDPAD_R_1_via1	Via1	Metal1	Metal2	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via2	Via2	Metal2	Metal3	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via3	Via3	Metal3	Metal4	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via4	Via4	Metal4	Metal5	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via5	Via5	Metal5	Metal6	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via6	Via6	Metal6	Metal7	16.0	BONDPAD.R.1
rule_BONDPAD_R_2_via7	Via7	Metal7	Metal8	4.0	BONDPAD.R.2
rule_BONDPAD_R_2_via8	Via8	Metal8	Metal9	4.0	BONDPAD.R.2

macro

Macro Table

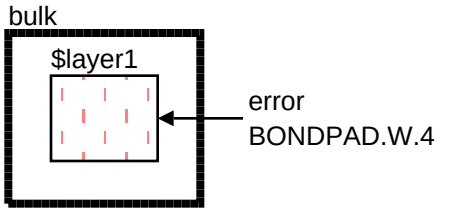
$layer1	$name1
rule_BONDPAD_SP_5_metal1	Metal1
rule_BONDPAD_SP_5_metal2	Metal2
rule_BONDPAD_SP_5_metal3	Metal3
rule_BONDPAD_SP_5_metal4	Metal4
rule_BONDPAD_SP_5_metal5	Metal5
rule_BONDPAD_SP_5_metal6	Metal6
rule_BONDPAD_SP_5_metal7	Metal7
rule_BONDPAD_SP_5_metal8	Metal8



macro

Macro Table

$layer1	$name1
rule_BONDPAD_W_4_metal1	Metal1
rule_BONDPAD_W_4_metal2	Metal2
rule_BONDPAD_W_4_metal3	Metal3
rule_BONDPAD_W_4_metal4	Metal4
rule_BONDPAD_W_4_metal5	Metal5
rule_BONDPAD_W_4_metal6	Metal6
rule_BONDPAD_W_4_metal7	Metal7
rule_BONDPAD_W_4_metal8	Metal8

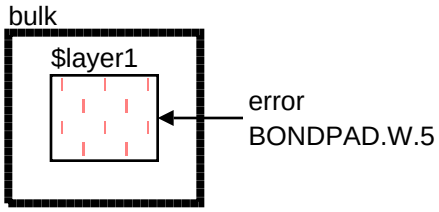


Bond Pad Design Rules (continued)

macro

Macro Table

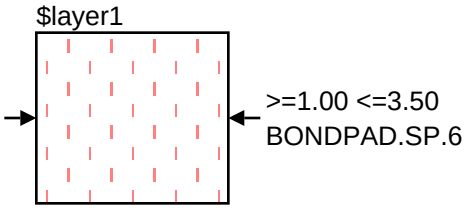
$layer1	$name1
rule_BONDPAD_W_5_metal1	Metal1
rule_BONDPAD_W_5_metal2	Metal2
rule_BONDPAD_W_5_metal3	Metal3
rule_BONDPAD_W_5_metal4	Metal4
rule_BONDPAD_W_5_metal5	Metal5
rule_BONDPAD_W_5_metal6	Metal6
rule_BONDPAD_W_5_metal7	Metal7
rule_BONDPAD_W_5_metal8	Metal8



macro

Macro Table

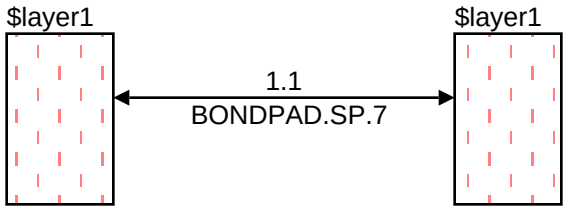
$layer1	$name1
bondpad_metal1_slot_on_edge	Metal1
bondpad_metal2_slot_on_edge	Metal2
bondpad_metal3_slot_on_edge	Metal3
bondpad_metal4_slot_on_edge	Metal4
bondpad_metal5_slot_on_edge	Metal5
bondpad_metal6_slot_on_edge	Metal6
bondpad_metal7_slot_on_edge	Metal7
bondpad_metal8_slot_on_edge	Metal8



macro

Macro Table

$layer1	$name1
bondpad_via1_array	Via1
bondpad_via2_array	Via2
bondpad_via3_array	Via3
bondpad_via4_array	Via4
bondpad_via5_array	Via5
bondpad_via6_array	Via6
bondpad_via7_array	Via7
bondpad_via8_array	Via8



CMOS Digital Electrical Parameters

Sheet Resistances

The units for sheet resistance are ohms/square

Global Parameters

R_metal8_9	0.02	Metal 8,9 sheet resistance	
R_metal2_7	0.06	Metal 2,3,4,5,6,7 sheet resistance	
R_metal1	0.08	Metal 1sheet resistance	
R_snpoly	10	Salicide N+ Poly sheet resistance	
R_sppoly	10	Salicide P+ Poly sheet resistance	
R_nsnpoly	100	Non-salicide N+ Poly sheet resistance	
R_nsppoly	400	Non-salicide P+ Poly sheet resistance	
R_snactive	10	Salicide N+ Oxide sheet resistance	
R_spactive	10	Salicide P+ Oxide sheet resistance	
R_nsnactive	100	Non-salicide N+ Oxide sheet resistance	
R_nspactive	150	Non-salicide P+ Oxide sheet resistance	
R_nwell	400	Nwell sheet resistance	
R_pwell	1600	Pwell sheet resistance	

Contact/Via Resistances

The units for sheet resistance are ohms/contact or ohms/via

Global Parameters

R_via7_8	0.35	Via 7,8 resistance	
R_via2_6	1.4	Via 2,3,4,5,6 resistance	
R_via1	1.4	Via 1 resistance	
R_metal1-contact	1	Metal 1 to Contact resistance	
R_poly-contact	10	Poly to Contact resistance	
R_nplus-contact	15	N+ Oxide to Contact resistance	
R_pplus-contact	15	P+ Oxide to Contact resistance	

Current Densities

The units for current density are ma/um

Global Parameters

L_metal8_9	8	Metal 8,9 current density	
L_metal1_7	2	Metal 1,2,3,4,5,6,7 current density	

Contact/Via Current Densities

The units for current density are ma/contact or ma/via

Global Parameters

I_via1_6	0.1	Via 1,2,3,4,5,6 current density	
I_Via7_8	0.8	Via 7,8 current density	
I_metal-contact-poly	0.1	Metal 1 Contact to Poly current density	
I_metal-contact-oxide	0.1	Metal 1 Contact to Oxide current density	

Layer and Dielectric Thickness

The units for layer and dielectric thickness are angstroms

Layer	Thickness (A)	Description
Pass2	7000	7.9
Pass1	10000	4.2
Metal 9	10000	Cu
IMD 8	6000	K = 4.2
Metal 8	10000	Cu
IMD 7	6000	K = 4.2
Metal 7	3600	Cu
IMD 6	3000	K = 2.9
Metal 6	3600	Cu
IMD 5	3000	K = 2.9
Metal 5	3600	Cu
IMD 4	3000	K = 2.9
Metal 4	3600	Cu
IMD 3	3000	K = 2.9
Metal 3	3600	Cu
IMD 2	3000	K = 2.9
Metal 2	3600	Cu
IMD 1	3000	K = 2.9
Metal 1	3000	Cu
ILD	3000	silicon dioxide K = 3.9
Poly	1500	
STI (FOX)	3500	silicon dioxide K = 3.9

1V PMOS

Tox	2.48nm	
Channel Concentration	1.20E+20	for MOS Vt fine tuning
D/S Surface Concentration	6.00E+20	
D/S Xj	60nm	
D/S Rsh	20 ohm/sq	
LDD Surface Concentration	6.00E+19	
LDD Xj	25nm	
LDD Rsh	500 ohm/sq	
Vto	-140mV	

1V NMOS

Tox	2.33nm	
Channel Concentration	6.0E+19	for MOS Vt fine tuning
D/S Surface Concentration	3.00E+20	
D/S Xj	60nm	
D/S Rsh	10 ohm/sq	
LDD Surface Concentration	3.00E+19	
LDD Xj	25nm	
LDD Rsh	250 ohm/sq	
Vto	170mV	

LP 1V PMOS

Tox	2.48nm	
Channel Concentration	1.20E+20	for MOS Vt fine tuning
D/S Surface Concentration	6.00E+20	
D/S Xj	60nm	
D/S Rsh	20 ohm/sq	
LDD Surface Concentration	6.00E+19	
LDD Xj	25nm	
LDD Rsh	500 ohm/sq	
Vto	-240mV	100mv more Vto to reduce leakage by 10x

LP 1V NMOS

Tox	2.33nm	
Channel Concentration	6.0E+19	for MOS Vt fine tuning
D/S Surface Concentration	3.00E+20	
D/S Xj	60nm	
D/S Rsh	10 ohm/sq	
LDD Surface Concentration	3.00E+19	
LDD Xj	25nm	
LDD Rsh	250 ohm/sq	
Vto	270mV	100mv more Vto to reduce leakage by 10x

I/O 2.5V PMOS

Tox	5.6nm	
Channel Concentration	1.20E+20	for MOS Vt fine tuning
D/S Surface Concentration	6.00E+20	
D/S Xj	60nm	
D/S Rsh	20 ohm/sq	
LDD Surface Concentration	6.00E+19	
LDD Xj	25nm	
LDD Rsh	500 ohm/sq	
Vto	-400mV	

I/O 2.5V NMOS

Tox	5.8nm	
Channel Concentration	6.0E+19	for MOS Vt fine tuning
D/S Surface Concentration	3.00E+20	
D/S Xj	60nm	
D/S Rsh	10 ohm/sq	
LDD Surface Concentration	3.00E+19	
LDD Xj	25nm	
LDD Rsh	250 ohm/sq	
Vto	450mV	

Key Fast-Slow Model Parameters

Fast Vto %	-10
Slow Vto %	10
Fast Tox %	-10
Slow Tox %	10
Fast Mobility %	-30
Slow Mobility %	30
Fast LDD Rsh %	-30
Slow LDD Rsh %	30

DF2 Layer Tables

CDB layers

Oxide	2	Oxide
Oxide_thk	4	Oxide_thk
Nwell	6	Nwell
Poly	10	Poly
Nhvt	11	Nhvt
Nimp	12	Nimp
Phvt	13	Phvt
Pimp	14	Pimp
Nzvt	15	Nzvt
SiProt	16	SiProt
Nburied	18	Nburied
Cont	20	Cont
Metal1	30	Metal1
Via1	32	Via1
Metal2	34	Metal2
Via2	36	Via2
Metal3	38	Metal3
Via3	40	Via3
Metal4	42	Metal4
Via4	44	Via4
Metal5	46	Metal5
Via5	48	Via5
Metal6	50	Metal6
Via6	52	Via6
Metal7	54	Metal7
Via7	56	Via7
Metal8	58	Metal8
Via8	60	Via8
Metal9	62	Metal9

CDB layers

Metal1_slot	71	M1slot
Metal2_slot	72	M2slot
Metal3_slot	73	M3slot
Metal4_slot	74	M4slot
Metal5_slot	75	M5slot
Metal6_slot	76	M6slot
Metal7_slot	77	M7slot
Metal8_slot	78	M8slot
Metal9_slot	79	M9slot

CDB layers

IND3dummy	114	IND3dum
ESDdummy	115	ESDdum

CDB layers

text	230	text

CDB layers

Psub	80	Psub
DIOdummy	82	DIOdum
PNPdummy	84	PNPdum
PWdummy	85	PWdummy
NPNdummy	86	NPNdum
IND2dummy	88	IND2dum
INDdummy	90	INDdum
BJTdum	92	BJTdum
Cap3dum	93	Cap3dum
Resdum	94	Resdum
Bondpad	95	Bondpad
Capdum	96	Capdum
CapMetal	97	CapMetal
ResWdum	98	ResWdum
M1Resdum	99	M1Resdum
M2Resdum	100	M2Resdum
M3Resdum	101	M3Resdum
M4Resdum	102	M4Resdum
M5Resdum	103	M5Resdum
M6Resdum	104	M6Resdum
M7Resdum	105	M7Resdum
M8Resdum	106	M8Resdum
M9Resdum	107	M9Resdum
VPNP2dum	108	VPNP2dum
VPNP5dum	109	VPNP5dum
VPNP10dum	110	VPNP10dum

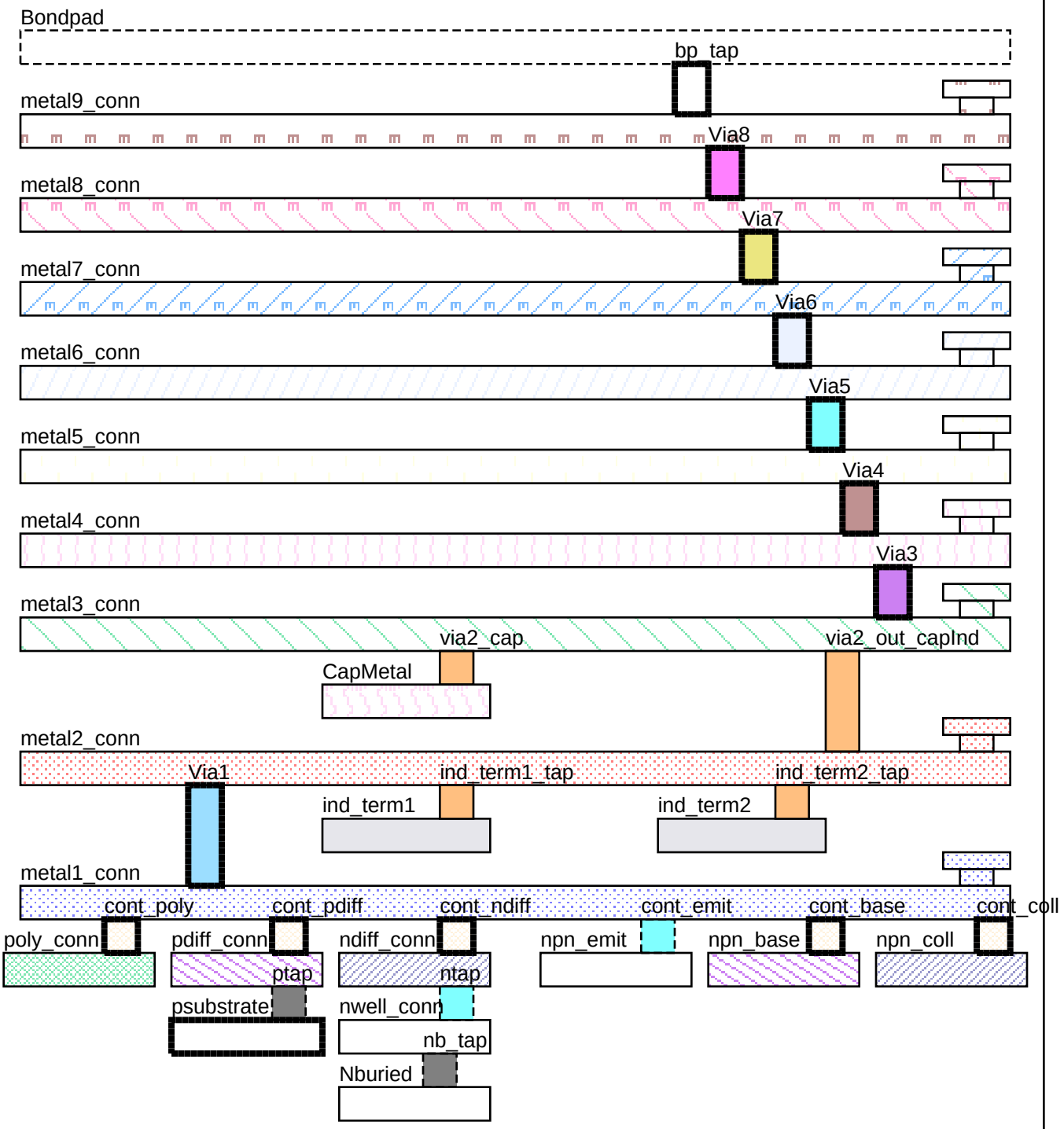
DF2 Layer Purposes Tables

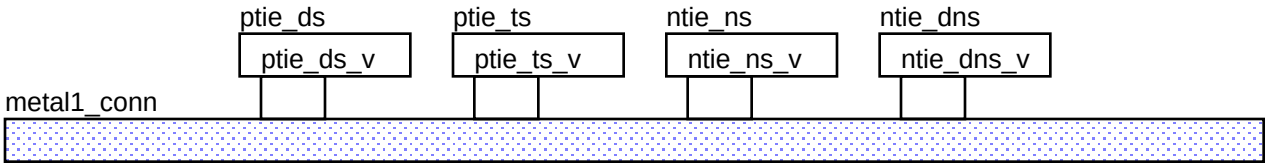
CDB purposes

slot	1	slt
port1	2	pt1
region	3	reg
grid	4	grd
ppath	5	pp0
ppath1	6	pp1
macro	7	mac
nwell	8	nwl
dnwell	9	dnw
ipwell	10	ipw
GeoShare	11	geo
port	12	pt0
fill	13	fil

Connectivity Definition

Connectivity




ptie_ds
ptie_ds_v
ptie_ts
ptie_ts_v
ntie_ns
ntie_ns_v
ntie_dns
ntie_dns_v
metal1_conn

$dt_Nimp	dummy	
$layer1	dummy	
$layer2	dummy	
$layer3	dummy	
BJTdum	input 15;0 df2order 103 packet zbip fillStyle outline	
Bondpad	input 36;0 df2order 96 (Bondpad drawing) packet pass	
Cap3dum	input 84;0 df2order 102 packet zcap fillStyle outline	
CapMetal	input 14;0 df2order 72 (CapMetal drawing) packet mcap	
Capdum	input 12;0 df2order 102 packet zcap fillStyle outline	
Cont	input 6;0 df2order 24 (Cont drawing) packet cw	via
DIOdummy	input 22;0 df2order 107 (DIOdummy drawing) packet zdiode	
ESDdummy	input 74;0 df2order 110 (ESDdummy drawing) packet esddum	
IND2dummy	input 17;0 df2order 100 (IND2dummy drawing) packet zind2	
IND3dummy	input 70;0 df2order 101 (IND3dummy drawing) packet zind3	
INDdummy	input 16;0 df2order 99 (INDdummy drawing) packet zind	
M1Resdum	input 75;0 (M1Resdum drawing) df2order 104 packet zrm1	
M2Resdum	input 76;0 (M2Resdum drawing) df2order 104 packet zrm2	
M3Resdum	input 77;0 (M3Resdum drawing) df2order 104 packet zrm3	
M4Resdum	input 78;0 (M4Resdum drawing) df2order 104 packet zrm4	
M5Resdum	input 79;0 (M5Resdum drawing) df2order 104 packet zrm5	
M6Resdum	input 80;0 (M6Resdum drawing) df2order 104 packet zrm6	
M7Resdum	input 81;0 (M7Resdum drawing) df2order 104 packet zrm7	
M8Resdum	input 82;0 (M8Resdum drawing) df2order 104 packet zrm8	
M9Resdum	input 83;0 (M9Resdum drawing) df2order 104 packet zrm9	
Metal1	Metal1_d_n or Metal1_p or Metal1_f	
Metal1_d	input 7;0 df2order 30 (Metal1 drawing) packet m1 Attach Text: 7;3 (Metal1 label)	
Metal1_d_n	if MergePinAndNet Metal1_d or Metal1_n else Metal1_d	
Metal1_f	input 7;5 df2order 81 (Metal1 fill) packet m1_fill	
Metal1_n	input 7;4 df2order 30 (Metal1 net) packet m1	
Metal1_p	input 7;1 df2order 30 (Metal1 pin) packet m1 Attach Text: 7;3 (Metal1 label)	
Metal1_slot	input 7;2 df2order 81 (Metal1 slot) packet m1_slot	
Metal1_slot_not_BP	Metal1_slot andnot (Bondpad size 3)	
Metal1_v	Metal1_p and Metal1_d	via
Metal2	Metal2_d_n or Metal2_p or Metal2_f	
Metal2_d	input 9;0 df2order 34 (Metal2 drawing) packet m2 Attach Text: 9;3 (Metal2 label)	

Metal2_d_n	if MergePinAndNet Metal2_d or Metal2_n else Metal2_d	
Metal2_f	input 9;5 df2order 82 (Metal2 fill) packet m2_fill	
Metal2_n	input 9;4 df2order 34 (Metal2 net) packet m2	
Metal2_p	input 9;1 df2order 34 (Metal2 pin) packet m2 Attach Text: 9;3 (Metal2 label)	
Metal2_slot	input 9;2 df2order 82 (Metal2 slot) packet m2_slot	
Metal2_slot_not_BP	Metal2_slot andnot (Bondpad size 3)	
Metal2_v	Metal2_p and Metal2_d	via
Metal3	Metal3_d_n or Metal3_p or Metal3_f	
Metal3_d	input 11;0 df2order 38 (Metal3 drawing) packet m3 Attach Text: 11;3 (Metal3 label)	
Metal3_d_n	if MergePinAndNet Metal3_d or Metal3_n else Metal3_d	
Metal3_f	input 11;5 df2order 83 (Metal3 fill) packet m3_fill	
Metal3_n	input 11;4 df2order 38 (Metal3 net) packet m3	
Metal3_p	input 11;1 df2order 38 (Metal3 pin) packet m3 Attach Text: 11;3 (Metal3 label)	
Metal3_slot	input 11;2 df2order 83 (Metal3 slot) packet m3_slot	
Metal3_slot_not_BP	Metal3_slot andnot (Bondpad size 3)	
Metal3_v	Metal3_p and Metal3_d	via
Metal4	Metal4_d_n or Metal4_p or Metal4_f	
Metal4_d	input 31;0 df2order 42 (Metal4 drawing) packet m4 Attach Text: 31;3 (Metal4 label)	
Metal4_d_n	if MergePinAndNet Metal4_d or Metal4_n else Metal4_d	
Metal4_f	input 31;5 df2order 84 (Metal4 fill) packet m4_fill	
Metal4_n	input 31;4 df2order 42 (Metal4 net) packet m4	
Metal4_p	input 31;1 df2order 42 (Metal4 pin) packet m4 Attach Text: 31;3 (Metal4 label)	
Metal4_slot	input 31;2 df2order 84 (Metal4 slot) packet m4_slot	
Metal4_slot_not_BP	Metal4_slot andnot (Bondpad size 3)	
Metal4_v	Metal4_p and Metal4_d	via
Metal5	Metal5_d_n or Metal5_p or Metal5_f	
Metal5_d	input 33;0 df2order 46 (Metal5 drawing) packet m5 Attach Text: 33;3 (Metal5 label)	
Metal5_d_n	if MergePinAndNet Metal5_d or Metal5_n else Metal5_d	
Metal5_f	input 33;5 df2order 85 (Metal5 fill) packet m5_fill	
Metal5_n	input 33;4 df2order 46 (Metal5 net) packet m5	
Metal5_p	input 33;1 df2order 46 (Metal5 pin) packet m5 Attach Text: 33;3 (Metal5 label)	
Metal5_slot	input 33;2 df2order 85 (Metal5 slot) packet m5_slot	
Metal5_slot_not_BP	Metal5_slot andnot (Bondpad size 3)	
Metal5_v	Metal5_p and Metal5_d	via
Metal6	Metal6_d_n or Metal6_p or Metal6_f	
Metal6_d	input 35;0 df2order 50 (Metal6 drawing) packet m6 Attach Text: 35;3 (Metal6 label)	
Metal6_d_n	if MergePinAndNet Metal6_d or Metal6_n else Metal6_d	
Metal6_f	input 35;5 df2order 86 (Metal6 fill) packet m6_fill	
Metal6_n	input 35;4 df2order 50 (Metal6 net) packet m6	
Metal6_p	input 35;1 df2order 50 (Metal6 pin) packet m6 Attach Text: 35;3 (Metal6 label)	
Metal6_slot	input 35;2 df2order 86 (Metal6 slot) packet m6_slot	

Metal6_slot_not_BP	Metal6_slot andnot (Bondpad size 3)	
Metal6_v	Metal6_p and Metal6_d	via
Metal7	Metal7_d_n or Metal7_p or Metal7_f	
Metal7_d	input 38;0 df2order 54 (Metal7 drawing) packet m7 Attach Text: 38;3 (Metal7 label)	
Metal7_d_n	if MergePinAndNet Metal7_d or Metal7_n else Metal7_d	
Metal7_f	input 38;5 df2order 87 (Metal7 fill) packet m7_fill	
Metal7_n	input 38;4 df2order 54 (Metal7 net) packet m7	
Metal7_p	input 38;1 df2order 54 (Metal7 pin) packet m7 Attach Text: 38;3 (Metal7 label)	
Metal7_slot	input 38;2 df2order 87 (Metal7 slot) packet m7_slot	
Metal7_slot_not_BP	Metal7_slot andnot (Bondpad size 3)	
Metal7_v	Metal7_p and Metal7_d	via
Metal8	Metal8_d_n or Metal8_p or Metal8_f	
Metal8_d	input 40;0 df2order 58 (Metal8 drawing) packet m8 Attach Text: 40;3 (Metal8 label)	
Metal8_d_n	if MergePinAndNet Metal8_d or Metal8_n else Metal8_d	
Metal8_f	input 40;5 df2order 88 (Metal8 fill) packet m8_fill	
Metal8_n	input 40;4 df2order 58 (Metal8 net) packet m8	
Metal8_p	input 40;1 df2order 58 (Metal8 pin) packet m8 Attach Text: 40;3 (Metal8 label)	
Metal8_slot	input 40;2 df2order 88 (Metal8 slot) packet m8_slot	
Metal8_slot_not_BP	Metal8_slot andnot (Bondpad size 3)	
Metal8_v	Metal8_p and Metal8_d	via
Metal9	Metal9_d_n or Metal9_p or Metal9_f	
Metal9_d	input 42;0 df2order 62 (Metal9 drawing) packet m9 Attach Text: 42;3 (Metal9 label)	
Metal9_d_n	if MergePinAndNet Metal9_d or Metal9_n else Metal9_d	
Metal9_f	input 42;5 df2order 89 (Metal9 fill) packet m9_fill	
Metal9_n	input 42;4 df2order 62 (Metal9 net) packet m9	
Metal9_p	input 42;1 df2order 62 (Metal9 pin) packet m9 Attach Text: 42;3 (Metal9 label)	
Metal9_slot	input 42;2 df2order 89 (Metal9 slot) packet m9_slot	
Metal9_slot_not_BP	Metal9_slot andnot (Bondpad size 3)	
Metal9_v	Metal9_p and Metal9_d	via
NOD	SNA Oxide and Nimp	
NPNdummy	input 20;0 df2order 105 (NPNdummy drawing) packet znpn	
Nburied	input 19;0 df2order 73 (Nburied drawing) packet npblk	
Nhvt	input 18;0 df2order 13 (Nhvt drawing) packet nhvt	
Nimp	input 4;0 df2order 14 (Nimp drawing) packet nplus	
Nwell	input 2;0 df2order 2 (Nwell drawing) packet nwell	
Nzvt	input 52;0 df2order 16 (Nzvt drawing) packet Nzvt	
Oxide	input 1;0 df2order 3 (Oxide drawing) packet tox	
Oxide_thk	input 24;0 df2order 4 (Oxide_thk drawing) packet Oxide_thk	
PNPdummy	input 21;0 df2order 105 (PNPdummy drawing) packet zpnp	

POD	SNA Oxide and Pimp	
PWdummy	input 85;0 df2order 85 (PWdummy drawing) packet zpw	
Phvt	input 23;0 df2order 15 (Phvt drawing) packet phvt	
Pimp	input 5;0 df2order 12 (Pimp drawing) packet pplus	
Poly	input 3;0 df2order 10 (Poly drawing) packet poly1	
Psub	input 25;0 (Psub drawing) df2order 75 packet psub	
ResWdum	input 71;0 df2order 103 (ResWdum drawing) packet zrwell	
Resdum	input 13;0 df2order 102 (Resdum drawing) packet zrpoly	
SiProt	input 72;0 df2order 18 (SiProt drawing) packet siprot	
VPNP2dum	input 60;0 df2order 103 packet zvpnp2 fillStyle outline	
VPNP5dum	input 61;0 df2order 103 packet zvpnp5 fillStyle outline	
VPNP10dum	input 62;0 df2order 103 packet zpnp10 fillStyle outline	
Via1	input 8;0 df2order 32 (Via1 drawing) packet v1	via
Via2	input 10;0 df2order 36 (Via2 drawing) packet v2	via
Via3	input 30;0 df2order 40 (Via3 drawing) packet v3	via
Via4	input 32;0 df2order 44 (Via4 drawing) packet v4	via
Via5	input 34;0 df2order 48 (Via5 drawing) packet v5	via
Via6	input 37;0 df2order 52 (Via6 drawing) packet v6	via
Via7	input 39;0 df2order 56 (Via7 drawing) packet v7	via
Via8	input 41;0 df2order 60 (Via8 drawing) packet v8	via
bondpad_metal1	(Metal1 and ((((((fill Metal1) enclose Bondpad) downUp 25.0) and (fill Metal1)) enclose Bondpad)))	
bondpad_metal1_filled	((((fill Metal1) enclose Bondpad) downUp 25.0) and (fill Metal1)) enclose Bondpad	
bondpad_metal1_slot	holes bondpad_metal1	
bondpad_metal1_slot_on_edge	(bondpad_metal1_slot buttOnly == 1 (bondpad_metal1_slot drcSep <= 2.5))	
bondpad_metal2	(Metal2 and ((((((fill Metal2) enclose Bondpad) downUp 25.0) and (fill Metal2)) enclose Bondpad)))	
bondpad_metal2_filled	((((fill Metal2) enclose Bondpad) downUp 25.0) and (fill Metal2)) enclose Bondpad	
bondpad_metal2_slot	holes bondpad_metal2	
bondpad_metal2_slot_on_edge	(bondpad_metal2_slot buttOnly == 1 (bondpad_metal2_slot drcSep <= 2.5))	
bondpad_metal3	(Metal3 and ((((((fill Metal3) enclose Bondpad) downUp 25.0) and (fill Metal3)) enclose Bondpad)))	
bondpad_metal3_filled	((((fill Metal3) enclose Bondpad) downUp 25.0) and (fill Metal3)) enclose Bondpad	
bondpad_metal3_slot	holes bondpad_metal3	
bondpad_metal3_slot_on_edge	(bondpad_metal3_slot buttOnly == 1 (bondpad_metal3_slot drcSep <= 2.5))	
bondpad_metal4	(Metal4 and ((((((fill Metal4) enclose Bondpad) downUp 25.0) and (fill Metal4)) enclose Bondpad)))	
bondpad_metal4_filled	((((fill Metal4) enclose Bondpad) downUp 25.0) and (fill Metal4)) enclose Bondpad	
bondpad_metal4_slot	holes bondpad_metal4	
bondpad_metal4_slot_on_edge	(bondpad_metal4_slot buttOnly == 1 (bondpad_metal4_slot drcSep <= 2.5))	
bondpad_metal5	(Metal5 and ((((((fill Metal5) enclose Bondpad) downUp 25.0) and (fill Metal5)) enclose Bondpad)))	

bondpad_metal5_filled	((((fill Metal5) enclose Bondpad) downUp 25.0) and (fill Metal5)) enclose Bondpad	
bondpad_metal5_slot	holes bondpad_metal5	
bondpad_metal5_slot_on_edge	(bondpad_metal5_slot buttOnly == 1 (bondpad_metal5_slot drcSep <= 2.5))	
bondpad_metal6	(Metal6 and ((((((fill Metal6) enclose Bondpad) downUp 25.0) and (fill Metal6)) enclose Bondpad)))	
bondpad_metal6_filled	((((fill Metal6) enclose Bondpad) downUp 25.0) and (fill Metal6)) enclose Bondpad	
bondpad_metal6_slot	holes bondpad_metal6	
bondpad_metal6_slot_on_edge	(bondpad_metal6_slot buttOnly == 1 (bondpad_metal6_slot drcSep <= 2.5))	
bondpad_metal7	(Metal7 and ((((((fill Metal7) enclose Bondpad) downUp 25.0) and (fill Metal7)) enclose Bondpad)))	
bondpad_metal7_filled	((((fill Metal7) enclose Bondpad) downUp 25.0) and (fill Metal7)) enclose Bondpad	
bondpad_metal7_slot	holes bondpad_metal7	
bondpad_metal7_slot_on_edge	(bondpad_metal7_slot buttOnly == 1 (bondpad_metal7_slot drcSep <= 2.5))	
bondpad_metal8	(Metal8 and ((((((fill Metal8) enclose Bondpad) downUp 25.0) and (fill Metal8)) enclose Bondpad)))	
bondpad_metal8_filled	((((fill Metal8) enclose Bondpad) downUp 25.0) and (fill Metal8)) enclose Bondpad	
bondpad_metal8_slot	holes bondpad_metal8	
bondpad_metal8_slot_on_edge	(bondpad_metal8_slot buttOnly == 1 (bondpad_metal8_slot drcSep <= 2.5))	
bondpad_metal9	(Metal9 and ((((((fill Metal9) enclose Bondpad) downUp 25.0) and (fill Metal9)) enclose Bondpad)))	
bondpad_metal9_filled	((((fill Metal9) enclose Bondpad) downUp 25.0) and (fill Metal9)) enclose Bondpad	
bondpad_sq	Remove the beveled Bondpad edges. Bondpad downUp 5.0	
bondpad_to_die_edge	Bondpad drcEncBy < 50.0 (bulk area > 100000.0)	
bondpad_via1_array	((Via1 and Bondpad) upDown 0.3)	
bondpad_via2_array	((Via2 and Bondpad) upDown 0.3)	
bondpad_via3_array	((Via3 and Bondpad) upDown 0.3)	
bondpad_via4_array	((Via4 and Bondpad) upDown 0.3)	
bondpad_via5_array	((Via5 and Bondpad) upDown 0.3)	
bondpad_via6_array	((Via6 and Bondpad) upDown 0.3)	
bondpad_via7_array	((Via7 and Bondpad) upDown 0.3)	
bondpad_via8_array	((Via8 and Bondpad) upDown 0.3)	
bp_tap	Bondpad and Metal9	via
bulk	substrate	
cont_antenna	cont_poly and Poly	
cont_array_zone	viak_array_zone(Cont 0.09 0.409 -0.09)	
cont_base	Cont and npn_base and pdiff	via
cont_coll	Cont and npn_coll andnot Psub	via
cont_diode	cont_ndiff or cont_pdiff	via
cont_emit	Cont and npn_emit	via
cont_ndiff	Cont and ndiff_conn	via
cont_pdiff	Cont and pdiff_conn	via
cont_poly	Cont and Poly	via
diff_diode	ndiff_conn or pdiff_conn	
gate	Poly and Oxide	device_recognition

ind_term1	INDdummy and IND2dummy	
ind_term1_tap	Metal2 and INDdummy and IND2dummy	via
ind_term2	INDdummy and IND3dummy	
ind_term2_tap	Metal2 and INDdummy and IND3dummy	via
metal1_conn	(Metal1 andnot Metal1_slot) andnot M1Resdum	
metal2_conn	(Metal2 andnot Metal2_slot) andnot M2Resdum	
metal3_conn	(Metal3 andnot Metal3_slot) andnot M3Resdum	
metal4_conn	(Metal4 andnot Metal4_slot) andnot M4Resdum	
metal5_conn	(Metal5 andnot Metal5_slot) andnot M5Resdum	
metal6_conn	(Metal6 andnot Metal6_slot) andnot M6Resdum	
metal7_conn	(Metal7 andnot Metal7_slot) andnot M7Resdum	
metal8_conn	(Metal8 andnot Metal8_slot) andnot M8Resdum	
metal9_conn	(Metal9 andnot Metal9_slot) andnot M9Resdum	
metal_2_6_stack	Metal2 and Metal3 and Metal4 and Metal5 and Metal6	
metal_2_7_stack	Metal2 and Metal3 and Metal4 and Metal5 and Metal6 and Metal7	
nact	SNA NOD andnot Nwell	
nactive	Nimp and Oxide	
nb_tap	Nburied and Nwell	soft_via
ndiff	(nactive andnot poly_conn)	
ndiff_conn	ndiff andnot Resdum andnot NPNdummy	
nmos_io_esd	(ndiff_conn and ESDdummy) buttOnly (Poly buttOnly (ndiff_conn connect Bondpad))	
npn_base	Psub and NPNdummy	
npn_coll	Nwell andnot ResWdum and NPNdummy	
npn_emit	ndiff andnot Resdum and NPNdummy and Psub	
nsd	ndiff_conn buttOnly Poly	
nsd_esd	nsd and ESDdummy	
ntap	Nwell and ndiff_conn	soft_via
ntap_esd	ntap and ESDdummy	
ntie	SNA NOD andnot nact	
ntie_dn	SNA ntie andnot ntie_n	
ntie_dns	SNA ntie_dn	
ntie_dns_v	SNA ntie_dns and metal1_conn	soft_via
ntie_n	SNA ntie andnot Nburied	
ntie_ns	SNA ntie_n	
ntie_ns_v	SNA ntie_ns and metal1_conn	soft_via

nw_dnw	SNA Nwell or Nburied	
nwell_conn	Nwell andnot ResWdum andnot NPNdummy	
nwell_in_od_res	((Nwell inside Oxide) cut SiProt) cut ResWdum	
nwellres	Nwell and ResWdum	
oxide_in_res	Oxide cut Resdum	
pactive	Pimp and Oxide	
pdiff	pactive andnot Poly	
pdiff_conn	pdiff andnot Resdum andnot NPNdummy	
pmos_io_esd	(pdiff_conn and ESDdummy) buttOnly (Poly buttOnly (pdiff_conn connect Bondpad))	
poly_conn	Poly andnot Resdum	
poly_in_res	Poly cut Resdum	
poly_on_field	Poly andnot Oxide	
poly_tap	poly_on_field and Poly	via
psd	pdiff_conn buttOnly Poly	
psd_esd	psd and ESDdummy	
psubstrate	(bulk andnot (Nburied and Nwell)) andnot (Psub andnot (Psub size -0.001)) andnot NPNdummy	
ptap	(pdiff_conn andnot Nwell)	soft_via
ptap_esd	ptap and ESDdummy	
ptie	SNA POD andnot Nwell	
ptie_d	SNA ptie andnot nw_dnw	
ptie_ds	SNA ptie_d	
ptie_ds_v	SNA ptie_ds and metal1_conn	soft_via
ptie_t	SNA ptie andnot ptie_d	
ptie_ts	SNA ptie_t	
ptie_ts_v	SNA ptie_ts and metal1_conn	soft_via
resdum_sz	Resdum or ((Resdum growEdges 0.001) andnot (Poly or Oxide))	
rule_BONDPAD_B_1_m1	(((((((fill Metal1) enclose Bondpad) downUp 25.0) and (fill Metal1)) enclose Bondpad)) andnot (((((((fill Metal1) enclose Bondpad) downUp 25.0) and (fill Metal1)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m2	(((((((fill Metal2) enclose Bondpad) downUp 25.0) and (fill Metal2)) enclose Bondpad)) andnot (((((((fill Metal2) enclose Bondpad) downUp 25.0) and (fill Metal2)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	

rule_BONDPAD_B_1_m3	(((((((fill Metal3) enclose Bondpad) downUp 25.0) and (fill Metal3)) enclose Bondpad)) andnot (((((((fill Metal3) enclose Bondpad) downUp 25.0) and (fill Metal3)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m4	(((((((fill Metal4) enclose Bondpad) downUp 25.0) and (fill Metal4)) enclose Bondpad)) andnot (((((((fill Metal4) enclose Bondpad) downUp 25.0) and (fill Metal4)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m5	(((((((fill Metal5) enclose Bondpad) downUp 25.0) and (fill Metal5)) enclose Bondpad)) andnot (((((((fill Metal5) enclose Bondpad) downUp 25.0) and (fill Metal5)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m6	(((((((fill Metal6) enclose Bondpad) downUp 25.0) and (fill Metal6)) enclose Bondpad)) andnot (((((((fill Metal6) enclose Bondpad) downUp 25.0) and (fill Metal6)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m7	(((((((fill Metal7) enclose Bondpad) downUp 25.0) and (fill Metal7)) enclose Bondpad)) andnot (((((((fill Metal7) enclose Bondpad) downUp 25.0) and (fill Metal7)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m8	(((((((fill Metal8) enclose Bondpad) downUp 25.0) and (fill Metal8)) enclose Bondpad)) andnot (((((((fill Metal8) enclose Bondpad) downUp 25.0) and (fill Metal8)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_B_1_m9	(((((((fill Metal9) enclose Bondpad) downUp 25.0) and (fill Metal9)) enclose Bondpad)) andnot (((((((fill Metal9) enclose Bondpad) downUp 25.0) and (fill Metal9)) enclose Bondpad)) drcSep <= 40.0)) vertex < 8	
rule_BONDPAD_L_1	bondpad_sq inside (bondpad_to_die_edge grow 68.0)	
rule_BONDPAD_R_1_via1	(((bondpad_metal1 and bondpad_metal2) enclose Via1) enclose < 16 Via1)	
rule_BONDPAD_R_1_via2	(((bondpad_metal2 and bondpad_metal3) enclose Via2) enclose < 16 Via2)	
rule_BONDPAD_R_1_via3	(((bondpad_metal3 and bondpad_metal4) enclose Via3) enclose < 16 Via3)	
rule_BONDPAD_R_1_via4	(((bondpad_metal4 and bondpad_metal5) enclose Via4) enclose < 16 Via4)	
rule_BONDPAD_R_1_via5	(((bondpad_metal5 and bondpad_metal6) enclose Via5) enclose < 16 Via5)	
rule_BONDPAD_R_1_via6	(((bondpad_metal6 and bondpad_metal7) enclose Via6) enclose < 16 Via6)	
rule_BONDPAD_R_2_via7	(((bondpad_metal7 and bondpad_metal8) enclose Via7) enclose < 4 Via7)	
rule_BONDPAD_R_2_via8	(((bondpad_metal8 and bondpad_metal9) enclose Via8) enclose < 4 Via8)	
rule_BONDPAD_SP_5_metal1	((bondpad_metal1_slot drcSep <= 2.5) andnot (bondpad_metal1_slot drcSep == 1.5))	

rule_BONDPAD_SP_5_metal2	((bondpad_metal2_slot drcSep <= 2.5) andnot (bondpad_metal2_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal3	((bondpad_metal3_slot drcSep <= 2.5) andnot (bondpad_metal3_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal4	((bondpad_metal4_slot drcSep <= 2.5) andnot (bondpad_metal4_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal5	((bondpad_metal5_slot drcSep <= 2.5) andnot (bondpad_metal5_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal6	((bondpad_metal6_slot drcSep <= 2.5) andnot (bondpad_metal6_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal7	((bondpad_metal7_slot drcSep <= 2.5) andnot (bondpad_metal7_slot drcSep == 1.5))	
rule_BONDPAD_SP_5_metal8	((bondpad_metal8_slot drcSep <= 2.5) andnot (bondpad_metal8_slot drcSep == 1.5))	
rule_BONDPAD_W_4_metal1	((bondpad_metal1_slot andnot (bondpad_metal1_slot drcWidth == 1.0)) andnot bondpad_metal1_slot_on_edge)	
rule_BONDPAD_W_4_metal2	((bondpad_metal2_slot andnot (bondpad_metal2_slot drcWidth == 1.0)) andnot bondpad_metal2_slot_on_edge)	
rule_BONDPAD_W_4_metal3	((bondpad_metal3_slot andnot (bondpad_metal3_slot drcWidth == 1.0)) andnot bondpad_metal3_slot_on_edge)	
rule_BONDPAD_W_4_metal4	((bondpad_metal4_slot andnot (bondpad_metal4_slot drcWidth == 1.0)) andnot bondpad_metal4_slot_on_edge)	
rule_BONDPAD_W_4_metal5	((bondpad_metal5_slot andnot (bondpad_metal5_slot drcWidth == 1.0)) andnot bondpad_metal5_slot_on_edge)	
rule_BONDPAD_W_4_metal6	((bondpad_metal6_slot andnot (bondpad_metal6_slot drcWidth == 1.0)) andnot bondpad_metal6_slot_on_edge)	
rule_BONDPAD_W_4_metal7	((bondpad_metal7_slot andnot (bondpad_metal7_slot drcWidth == 1.0)) andnot bondpad_metal7_slot_on_edge)	
rule_BONDPAD_W_4_metal8	((bondpad_metal8_slot andnot (bondpad_metal8_slot drcWidth == 1.0)) andnot bondpad_metal8_slot_on_edge)	
rule_BONDPAD_W_5_metal1	((((bondpad_metal1_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal1_filled andnot (bondpad_metal1_slot or (bondpad_metal1_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal2	((((bondpad_metal2_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal2_filled andnot (bondpad_metal2_slot or (bondpad_metal2_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal3	((((bondpad_metal3_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal3_filled andnot (bondpad_metal3_slot or (bondpad_metal3_slot drcSep <= 10.0))) drcWidth == 5.0))	

rule_BONDPAD_W_5_metal4	((((bondpad_metal4_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal4_filled andnot (bondpad_metal4_slot or (bondpad_metal4_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal5	((((bondpad_metal5_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal5_filled andnot (bondpad_metal5_slot or (bondpad_metal5_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal6	((((bondpad_metal6_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal6_filled andnot (bondpad_metal6_slot or (bondpad_metal6_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal7	((((bondpad_metal7_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal7_filled andnot (bondpad_metal7_slot or (bondpad_metal7_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_BONDPAD_W_5_metal8	((((bondpad_metal8_filled size -25.0) size 20.0) growEdges 5.0) outside ((bondpad_metal8_filled andnot (bondpad_metal8_slot or (bondpad_metal8_slot drcSep <= 10.0))) drcWidth == 5.0))	
rule_Bondpad_Missing_M1	Bondpad notInteract Metal1	
rule_Bondpad_Missing_M2	Bondpad notInteract Metal2	
rule_Bondpad_Missing_M3	Bondpad notInteract Metal3	
rule_Bondpad_Missing_M4	Bondpad notInteract Metal4	
rule_Bondpad_Missing_M5	Bondpad notInteract Metal5	
rule_Bondpad_Missing_M6	Bondpad notInteract Metal6	
rule_Bondpad_Missing_M7	Bondpad notInteract Metal7	
rule_Bondpad_Missing_M8	Bondpad notInteract Metal8	
rule_Bondpad_Missing_M9	Bondpad notInteract Metal9	
rule_Bondpad_Missing_V1	(((((Bondpad size -3) and Metal1) and Metal2)) andnot (Metal1_slot or Metal2_slot)) notInteract Via1	
rule_Bondpad_Missing_V2	(((((Bondpad size -3) and Metal2) and Metal3)) andnot (Metal2_slot or Metal3_slot)) notInteract Via2	
rule_Bondpad_Missing_V3	(((((Bondpad size -3) and Metal3) and Metal4)) andnot (Metal3_slot or Metal4_slot)) notInteract Via3	
rule_Bondpad_Missing_V4	(((((Bondpad size -3) and Metal4) and Metal5)) andnot (Metal4_slot or Metal5_slot)) notInteract Via4	
rule_Bondpad_Missing_V5	(((((Bondpad size -3) and Metal5) and Metal6)) andnot (Metal5_slot or Metal6_slot)) notInteract Via5	
rule_Bondpad_Missing_V6	(((((Bondpad size -3) and Metal6) and Metal7)) andnot (Metal6_slot or Metal7_slot)) notInteract Via6	

rule_Bondpad_Missing_V7	(((((Bondpad size -3) and Metal7) and Metal8)) andnot (Metal7_slot or Metal8_slot)) notInteract Via7	
rule_Bondpad_Missing_V8	(((((Bondpad size -3) and Metal8) and Metal9)) andnot (Metal8_slot or Metal9_slot)) notInteract Via8	
rule_ESD_4_nmos	(nsd_esd buttOnly == 1 Poly) andnot ((ndiff_conn connect Bondpad) or (ndiff_conn connect psubstrate))	
rule_ESD_4_pmos	(psd_esd buttOnly == 1 Poly) andnot ((pdiff_conn connect Bondpad) or (pdiff_conn connect nwell_conn))	
rule_ESD_5	(Oxide cut nsd_esd) andnot (holes ptap_esd)	
rule_ESD_6	(Oxide cut psd_esd) andnot (holes ntap_esd)	
rule_ESD_7_nmos	ptap_esd buttOnly nsd_esd	
rule_ESD_7_pmos	ntap_esd buttOnly psd_esd	
rule_ESD_8_nmos	((nsd_esd buttOnly == 2 Poly) andnot ((ndiff_conn connect Bondpad) or (ndiff_conn connect psubstrate))) outside SiProt	
rule_ESD_8_pmos	((psd_esd buttOnly == 2 Poly) andnot ((pdiff_conn connect Bondpad) or (pdiff_conn connect psubstrate))) outside SiProt	
rule_NBL_X_1	Nburied outside (holes Nwell)	
rule_NHVT_X_1	(Oxide and Nhvt) xor Nhvt	
rule_NZVT_O_1	((Oxide interact Nzvt) size 0.3) xor Nzvt	
rule_NZVT_X_4	Nzvt interact > 1 Oxide	
rule_OXIDER_X_2	(Oxide cut Resdum) outside SiProt	
rule_OXIDE_L_1_L_2	((Oxide andnot (Cont sizeWithin 11.0 0.1 Oxide)) interact (Oxide andnot (Oxide downUp 0.09))) buttOnly (Cont sizeWithin 11.0 0.1 Oxide)	
rule_PHVT_X_1	(Oxide and Phvt) xor Phvt	
rule_POLY_SE_3	((Poly andnot (Cont sizeWithin 12.5 0.2 Poly)) buttOnly == 2 (Cont sizeWithin 12.5 0.2 Poly)) andnot (Poly downUp 0.07)	
rule_VIA1_X_1	viak_x_1_macro_b(via1_x_1 Metal1 Metal2) andnot rule_VIA1_X_2	
rule_VIA1_X_2	viak_x_2_macro_b(via1_x_2 Metal1 Metal2)	
rule_VIA2_X_1	viak_x_1_macro_b(via2_x_1 Metal2 Metal3) andnot rule_VIA2_X_2	
rule_VIA2_X_2	viak_x_2_macro_b(via2_x_2 Metal2 Metal3)	
rule_VIA3_X_1	viak_x_1_macro_b(via3_x_1 Metal3 Metal4) andnot rule_VIA3_X_2	
rule_VIA3_X_2	viak_x_2_macro_b(via3_x_2 Metal3 Metal4)	
rule_VIA4_X_1	viak_x_1_macro_b(via4_x_1 Metal4 Metal5) andnot rule_VIA4_X_2	
rule_VIA4_X_2	viak_x_2_macro_b(via4_x_2 Metal4 Metal5)	
rule_VIA5_X_1	viak_x_1_macro_b(via5_x_1 Metal5 Metal6) andnot rule_VIA5_X_2	
rule_VIA5_X_2	viak_x_2_macro_b(via5_x_2 Metal5 Metal6)	
rule_VIA6_X_1	viak_x_1_macro_b(via6_x_1 Metal6 Metal7) andnot rule_VIA6_X_2	
rule_VIA6_X_2	viak_x_2_macro_b(via6_x_2 Metal6 Metal7)	
rule_VIAk_X_3_X_4a	metal_2_6_stack enclose == 1 via_1_5_stack	
rule_VIAk_X_3_X_4b	metal_2_7_stack enclose == 1 via_2_6_stack	
siprot_in_nwell_res	SiProt cut nwell_in_od_res	
text	input	
via1_array_zone	viak_array_zone(Via1 0.11 0.499 -0.11)	
via1_x_1	viak_x_1_macro_a(Via1 Metal1 Metal2)	
via1_x_2	viak_x_2_macro_a(Via1 Metal1 Metal2)	

via2_array_zone	viak_array_zone(Via2 0.11 0.499 -0.11)	
via2_cap	Via2 and CapMetal	via
via2_out_capInd	Via2 and Metal2 andnot (CapMetal or INDdummy)	via
via2_x_1	viak_x_1_macro_a(Via2 Metal2 Metal3)	
via2_x_2	viak_x_2_macro_a(Via2 Metal2 Metal3)	
via3_array_zone	viak_array_zone(Via3 0.11 0.499 -0.11)	
via3_x_1	viak_x_1_macro_a(Via3 Metal3 Metal4)	
via3_x_2	viak_x_2_macro_a(Via3 Metal3 Metal4)	
via4_array_zone	viak_array_zone(Via4 0.11 0.499 -0.11)	
via4_x_1	viak_x_1_macro_a(Via4 Metal4 Metal5)	
via4_x_2	viak_x_2_macro_a(Via4 Metal4 Metal5)	
via5_array_zone	viak_array_zone(Via5 0.11 0.499 -0.11)	
via5_x_1	viak_x_1_macro_a(Via5 Metal5 Metal6)	
via5_x_2	viak_x_2_macro_a(Via5 Metal5 Metal6)	
via6_array_zone	viak_array_zone(Via6 0.11 0.499 -0.11)	
via6_x_1	viak_x_1_macro_a2(Via6 Metal6 Metal7)	
via6_x_2	viak_x_2_macro_a2(Via6 Metal6 Metal7)	
via_1_5_stack	Via1 and Via2 and Via3 and Via4 and Via5	
via_2_6_stack	Via2 and Via3 and Via4 and Via5 and Via6	
viak_array_zone	This macro will find array zones for layer1. macro (layer1 value1 value2 value3) ((layer1 size value1) downUp value2) size value3	via
viak_x_1_macro_a	This macro will find vias that are on metal wider than 0.40um. macro (via metalx metaly) via and ((metalx downUp 0.20) or (metaly downUp 0.20))	
viak_x_1_macro_a2	This macro will find vias that are on metal wider than 0.40um on the bottom and 1.6um on the top. macro (via metalx metaly) via and ((metalx downUp 0.20) or (metaly downUp 0.80))	
viak_x_1_macro_b	This macro will find any metal overlaps with via that have only one via. macro (via metalx metaly) ((metalx and metaly) enclose via) outside (((via size 0.15) and (metalx and metaly)) enclose > 1 via) outside (((via size 0.30) and (metalx and metaly)) enclose > 3 via)	
viak_x_2_macro_a	This macro will find vias that are on metal wider than 1.0um. macro (via metalx metaly) via and ((metalx downUp 0.50) or (metaly downUp 0.50))	
viak_x_2_macro_a2	This macro will find vias that are on metal wider than 1.0um on the bottom and 4.0um on the top. macro (via metalx metaly) via and ((metalx downUp 0.50) or (metaly downUp 2.00))	

viak_x_2_macro_b	This macro will find any metal overlaps with via that have only one via. macro (via metalx metaly) ((metalx and metaly) enclose via) outside (((via size 0.15) and (metalx and metaly)) enclose > 3 via) outside (((via size 0.30) and (metalx and metaly)) enclose > 8 via)	

ANT.1	Field Poly area to gate area ratio must be <= 275.0
ANT.2	Field Poly perimeter to gate area ratio must be <= 550.0
ANT.3	Poly Contact area to gate area ratio must be <= 15.0
ANT.4.M1	Metal1 area / (gate area + 2*diff area) ratio must be <= 475.0
ANT.4.M2	Metal2 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M3	Metal3 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M4	Metal4 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M5	Metal5 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M6	Metal6 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M7	Metal7 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M8	Metal8 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.4.M9	Metal9 area to (gate area + 2*diff_diode.area) ratio must be <= 475.0
ANT.5.V1	Via1 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V2	Via2 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V3	Via3 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V4	Via4 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V5	Via5 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V6	Via6 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V7	Via7 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.5.V8	Via8 area to (gate area + 2*diff_diode.area) ratio must be <= 25.0
ANT.6.M2	Cumulative Metal1 through Metal2 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M3	Cumulative Metal1 through Metal3 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M4	Cumulative Metal1 through Metal4 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M5	Cumulative Metal1 through Metal5 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M6	Cumulative Metal1 through Metal6 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M7	Cumulative Metal1 through Metal7 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M8	Cumulative Metal1 through Metal8 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
ANT.6.M9	Cumulative Metal1 through Metal9 area to (gate area + 2*diff_diode.area) ratio must be <= 1200.0
BONDPAD.B.1	Bondpad Metal1 must have bevelled corners
BONDPAD.B.1	Bondpad Metal2 must have bevelled corners
BONDPAD.B.1	Bondpad Metal3 must have bevelled corners
BONDPAD.B.1	Bondpad Metal4 must have bevelled corners
BONDPAD.B.1	Bondpad Metal5 must have bevelled corners
BONDPAD.B.1	Bondpad Metal6 must have bevelled corners
BONDPAD.B.1	Bondpad Metal7 must have bevelled corners
BONDPAD.B.1	Bondpad Metal8 must have bevelled corners
BONDPAD.B.1	Bondpad Metal9 must have bevelled corners
BONDPAD.B.1	Bondpad Metal1 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal2 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal3 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal4 beveled segments must be >= 1.8 um and <= 3.2 um

BONDPAD.B.1	Bondpad Metal5 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal6 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal7 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal8 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.B.1	Bondpad Metal9 beveled segments must be >= 1.8 um and <= 3.2 um
BONDPAD.E.1	Metal1 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal2 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal3 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal4 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal5 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal6 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal7 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal8 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.1	Metal9 to Bondpad enclosure must be >= 2.0 um
BONDPAD.E.2	Bondpad Metal1 to Via1 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal2 to Via2 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal3 to Via3 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal4 to Via4 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal5 to Via5 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal6 to Via6 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal2 to Via1 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal3 to Via2 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal4 to Via3 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal5 to Via4 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal6 to Via5 enclosure must be >= 0.05 um
BONDPAD.E.2	Bondpad Metal7 to Via6 enclosure must be >= 0.05 um
BONDPAD.E.3	Bondpad Metal7 to Via7 enclosure must be >= 0.09 um
BONDPAD.E.3	Bondpad Metal8 to Via8 enclosure must be >= 0.09 um
BONDPAD.E.3	Bondpad Metal8 to Via7 enclosure must be >= 0.09 um
BONDPAD.E.3	Bondpad Metal9 to Via8 enclosure must be >= 0.09 um
BONDPAD.L.1	Bondpad length must be >= 68.0 um
BONDPAD.O.1	Bondpads must contain Metal 1
BONDPAD.O.1	Bondpads must contain Metal 2
BONDPAD.O.1	Bondpads must contain Metal 3
BONDPAD.O.1	Bondpads must contain Metal 4
BONDPAD.O.1	Bondpads must contain Metal 5
BONDPAD.O.1	Bondpads must contain Metal 6
BONDPAD.O.1	Bondpads must contain Metal 7
BONDPAD.O.1	Bondpads must contain Metal 8
BONDPAD.O.1	Bondpads must contain Metal 9
BONDPAD.O.2	Bondpad Metal1/Metal2 intersection must contain Via 1
BONDPAD.O.2	Bondpad Metal2/Metal3 intersection must contain Via 2
BONDPAD.O.2	Bondpad Metal3/Metal4 intersection must contain Via 3
BONDPAD.O.2	Bondpad Metal4/Metal5 intersection must contain Via 4
BONDPAD.O.2	Bondpad Metal5/Metal6 intersection must contain Via 5
BONDPAD.O.2	Bondpad Metal6/Metal7 intersection must contain Via 6
BONDPAD.O.2	Bondpad Metal7/Metal8 intersection must contain Via 7
BONDPAD.O.2	Bondpad Metal8/Metal9 intersection must contain Via 8

BONDPAD.R.1	Minimum Bondpad Via1 inside Metal1 to Metal2 crossing must be >= 16.0
BONDPAD.R.1	Minimum Bondpad Via2 inside Metal2 to Metal3 crossing must be >= 16.0
BONDPAD.R.1	Minimum Bondpad Via3 inside Metal3 to Metal4 crossing must be >= 16.0
BONDPAD.R.1	Minimum Bondpad Via4 inside Metal4 to Metal5 crossing must be >= 16.0
BONDPAD.R.1	Minimum Bondpad Via5 inside Metal5 to Metal6 crossing must be >= 16.0
BONDPAD.R.1	Minimum Bondpad Via6 inside Metal6 to Metal7 crossing must be >= 16.0
BONDPAD.R.2	Minimum Bondpad Via7 inside Metal7 to Metal8 crossing must be >= 4.0
BONDPAD.R.2	Minimum Bondpad Via8 inside Metal8 to Metal9 crossing must be >= 4.0
BONDPAD.SP.1	Bondpad to Bondpad spacing must be >= 8.0 um
BONDPAD.SP.2	Bondpad Metal1 to Metal1 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal2 to Metal2 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal3 to Metal3 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal4 to Metal4 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal5 to Metal5 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal6 to Metal6 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal7 to Metal7 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal8 to Metal8 spacing must be >= 3.0 um
BONDPAD.SP.2	Bondpad Metal9 to Metal9 spacing must be >= 3.0 um
BONDPAD.SP.3	Bondpad Via1 to Bondpad Via1 spacing must be >= 0.22 um
BONDPAD.SP.3	Bondpad Via2 to Bondpad Via2 spacing must be >= 0.22 um
BONDPAD.SP.3	Bondpad Via3 to Bondpad Via3 spacing must be >= 0.22 um
BONDPAD.SP.3	Bondpad Via4 to Bondpad Via4 spacing must be >= 0.22 um
BONDPAD.SP.3	Bondpad Via5 to Bondpad Via5 spacing must be >= 0.22 um
BONDPAD.SP.3	Bondpad Via6 to Bondpad Via6 spacing must be >= 0.22 um
BONDPAD.SP.4	Bondpad Via7 to Bondpad Via7 spacing must be >= 0.54 um
BONDPAD.SP.4	Bondpad Via8 to Bondpad Via8 spacing must be >= 0.54 um
BONDPAD.SP.5	Bondpad Metal1 slot to Bondpad Metal1 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal2 slot to Bondpad Metal2 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal3 slot to Bondpad Metal3 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal4 slot to Bondpad Metal4 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal5 slot to Bondpad Metal5 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal6 slot to Bondpad Metal6 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal7 slot to Bondpad Metal7 slot spacing must be == 1.50
BONDPAD.SP.5	Bondpad Metal8 slot to Bondpad Metal8 slot spacing must be == 1.50
BONDPAD.SP.6	Bondpad Metal1 to Bondpad Metal1 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal2 to Bondpad Metal2 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal3 to Bondpad Metal3 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal4 to Bondpad Metal4 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal5 to Bondpad Metal5 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal6 to Bondpad Metal6 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.6	Bondpad Metal7 to Bondpad Metal7 spacing across first slot must be >= 1.00 um and <= 3.50 um

BONDPAD.SP.6	Bondpad Metal8 to Bondpad Metal8 spacing across first slot must be >= 1.00 um and <= 3.50 um
BONDPAD.SP.7	Bondpad Via1 array to Bondpad Via1 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via2 array to Bondpad Via2 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via3 array to Bondpad Via3 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via4 array to Bondpad Via4 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via5 array to Bondpad Via5 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via6 array to Bondpad Via6 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via7 array to Bondpad Via7 array spacing must be >= 1.1 um
BONDPAD.SP.7	Bondpad Via8 array to Bondpad Via8 array spacing must be >= 1.1 um
BONDPAD.W.1	Bondpad width must be >= 52.0 um
BONDPAD.W.4	Bondpad Metal1 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal2 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal3 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal4 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal5 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal6 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal7 slot width must be == 1.00
BONDPAD.W.4	Bondpad Metal8 slot width must be == 1.00
BONDPAD.W.5	Bondpad Metal1 outside Metal1 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal2 outside Metal2 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal3 outside Metal3 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal4 outside Metal4 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal5 outside Metal5 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal6 outside Metal6 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal7 outside Metal7 ring width must be == 5.00
BONDPAD.W.5	Bondpad Metal8 outside Metal8 ring width must be == 5.00
CONT.E.1	Oxide to Cont enclosure must be >= 0.06 um
CONT.E.2	Poly to Cont enclosure must be >= 0.04 um
CONT.E.3	Poly to Cont enclosure on at least two opposite sides must be >= 0.06 um
CONT.E.4	Nimp to Cont enclosure must be >= 0.06 um
CONT.E.4	Pimp to Cont enclosure must be >= 0.06 um
CONT.SE.1	Cont to gate spacing must be >= 0.10 um
CONT.SE.1.DFM	Cont to gate spacing must be >= 0.12 um for DFM
CONT.SE.2	Cont to 2.5V gate spacing must be >= 0.12 um
CONT.SE.2.DFM	Cont to 2.5V gate spacing must be >= 0.14 um for DFM
CONT.SE.3	Poly Cont to Oxide spacing must be >= 0.12 um
CONT.SE.3.DFM	Poly Cont to Oxide spacing must be >= 0.14 um for DFM
CONT.SE.4	Poly Cont to Oxide spacing must be >= 0.14 um
CONT.SE.4.DFM	Poly Cont to Oxide spacing must be >= 0.16 um for DFM
CONT.SP.1	Cont to Cont spacing must be >= 0.14 um
CONT.SP.2	Cont to Cont (in array) spacing must be >= 0.16 um
CONT.W.1	Cont shapes must be 0.12x0.12 rectangles
CONT.X.1	Cont on gate is NOT allowed
CONT.X.2	Nimp edge is NOT allowed on Oxide Cont
CONT.X.2	Pimp edge is NOT allowed on Oxide Cont
CONT.X.3	Cont must be covered by Oxide or Poly
ESD.1	ESD gate width must be >= 15.0 um and <= 65.0 um

ESD.4	N+ source should connect to Pad or Bulk
ESD.4	P+ source should connect to Pad or Nwell
ESD.5	NMOS I/O and ESD devices must be inside P+ rings
ESD.6	PMOS I/O and ESD devices must be inside N+ rings
ESD.7	P+ taps can NOT butt NMOS I/O and ESD devices
ESD.7	N+ taps can NOT butt PMOS I/O and ESD devices
ESD.8	N+ drains must be non-salicided (except Contact area)
ESD.8	P+ drains must be non-salicided (except Contact area)
ESD.11	SiProt to Poly gate overlap must be >= 0.05 um
ESD.12	SiProt to Poly gate enclosure must be >= 1.8 um
ESD.13	SiProt to Oxide overlap must be >= 1.8 um
ESD.14	ESD gate length must be == 0.3 um
ESD.15	Poly gate to Cont spacing must be >= 0.25 um
LATCHUP.1	P+SD to NW tap spacing must be <= 25.0 um
LATCHUP.2	N+SD to Psub tap spacing must be <= 25.0 um
LATCHUP.3	NMOS (I/O or ESD) to PMOS (I/O or ESD) spacing must be >= 18.0 um
LATCHUP.3	NMOS (I/O or ESD) to PMOS (I/O or ESD) spacing must be >= 50.0 um when not blocked by a double guard ring
METAL1.A.1	Metal1 area must be >= 0.07 um
METAL1.D.1	Metal1 density must be >= 20% <= 65%
METAL1.D.2	Metal1 density must be <= 60%
METAL1.E.1	Metal1 to Cont enclosure must be >= 0.00 um
METAL1.E.2	Metal1 to Cont enclosure on opposite sides must be >= 0.06 um
METAL1.L.1	Metal1 non-90 degree segments must be >= 0.18 um
METAL1.SP.1.1	Metal1 to Metal1 spacing must be >= 0.12 um
METAL1.SP.1.2	Metal1 to Metal1 spacing must be >= 0.18 um
METAL1.SP.1.3	Metal1 to Metal1 spacing must be >= 0.50 um
METAL1.SP.1.4	Metal1 to Metal1 spacing must be >= 0.90 um
METAL1.SP.1.5	Metal1 to Metal1 spacing must be >= 1.50 um
METAL1.SP.1.6	Metal1 to Metal1 spacing must be >= 2.50 um
METAL1.SP.2	Metal1 to bent Metal1 spacing must be >= 0.16 um
METAL1.W.1	Metal1 width must be >= 0.12 um
METAL1.W.2	Metal1 width must be <= 12.0 um
METAL1.W.3	Bent Metal1 (45 degree angle) width must be >= 0.14
METAL2.A.1	Metal2 area must be >= 0.08 um
METAL2.D.1	Metal2 density must be >= 20% <= 65%
METAL2.D.2	Metal2 density must be <= 60%
METAL2.E.1	Metal2 to Via1 enclosure must be >= 0.005 um
METAL2.E.2	Metal2 to Via1 enclosure on opposite sides must be >= 0.06 um
METAL2.L.1	Metal2 non-90 degree segments must be >= 0.20 um
METAL2.SP.1.1	Metal2 to Metal2 spacing must be >= 0.14 um
METAL2.SP.1.2	Metal2 to Metal2 spacing must be >= 0.20 um
METAL2.SP.1.3	Metal2 to Metal2 spacing must be >= 0.50 um
METAL2.SP.1.4	Metal2 to Metal2 spacing must be >= 0.90 um
METAL2.SP.1.5	Metal2 to Metal2 spacing must be >= 1.50 um
METAL2.SP.1.6	Metal2 to Metal2 spacing must be >= 2.50 um
METAL2.SP.2	Metal2 to bent Metal2 spacing must be >= 0.18 um
METAL2.W.1	Metal2 width must be >= 0.14 um

METAL2.W.2	Metal2 width must be <= 12.0 um
METAL2.W.3	Bent Metal2 (45 degree angle) width must be >= 0.16
METAL3.A.1	Metal3 area must be >= 0.08 um
METAL3.D.1	Metal3 density must be >= 20% <= 65%
METAL3.D.2	Metal3 density must be <= 60%
METAL3.E.1	Metal3 to Via2 enclosure must be >= 0.005 um
METAL3.E.2	Metal3 to Via2 enclosure on opposite sides must be >= 0.06 um
METAL3.L.1	Metal3 non-90 degree segments must be >= 0.20 um
METAL3.SP.1.1	Metal3 to Metal3 spacing must be >= 0.14 um
METAL3.SP.1.2	Metal3 to Metal3 spacing must be >= 0.20 um
METAL3.SP.1.3	Metal3 to Metal3 spacing must be >= 0.50 um
METAL3.SP.1.4	Metal3 to Metal3 spacing must be >= 0.90 um
METAL3.SP.1.5	Metal3 to Metal3 spacing must be >= 1.50 um
METAL3.SP.1.6	Metal3 to Metal3 spacing must be >= 2.50 um
METAL3.SP.2	Metal3 to bent Metal3 spacing must be >= 0.18 um
METAL3.W.1	Metal3 width must be >= 0.14 um
METAL3.W.2	Metal3 width must be <= 12.0 um
METAL3.W.3	Bent Metal3 (45 degree angle) width must be >= 0.16
METAL4.A.1	Metal4 area must be >= 0.08 um
METAL4.D.1	Metal4 density must be >= 20% <= 65%
METAL4.D.2	Metal4 density must be <= 60%
METAL4.E.1	Metal4 to Via3 enclosure must be >= 0.005 um
METAL4.E.2	Metal4 to Via3 enclosure on opposite sides must be >= 0.06 um
METAL4.L.1	Metal4 non-90 degree segments must be >= 0.20 um
METAL4.SP.1.1	Metal4 to Metal4 spacing must be >= 0.14 um
METAL4.SP.1.2	Metal4 to Metal4 spacing must be >= 0.20 um
METAL4.SP.1.3	Metal4 to Metal4 spacing must be >= 0.50 um
METAL4.SP.1.4	Metal4 to Metal4 spacing must be >= 0.90 um
METAL4.SP.1.5	Metal4 to Metal4 spacing must be >= 1.50 um
METAL4.SP.1.6	Metal4 to Metal4 spacing must be >= 2.50 um
METAL4.SP.2	Metal4 to bent Metal4 spacing must be >= 0.18 um
METAL4.W.1	Metal4 width must be >= 0.14 um
METAL4.W.2	Metal4 width must be <= 12.0 um
METAL4.W.3	Bent Metal4 (45 degree angle) width must be >= 0.16
METAL5.A.1	Metal5 area must be >= 0.08 um
METAL5.D.1	Metal5 density must be >= 20% <= 65%
METAL5.D.2	Metal5 density must be <= 60%
METAL5.E.1	Metal5 to Via4 enclosure must be >= 0.005 um
METAL5.E.2	Metal5 to Via4 enclosure on opposite sides must be >= 0.06 um
METAL5.L.1	Metal5 non-90 degree segments must be >= 0.20 um
METAL5.SP.1.1	Metal5 to Metal5 spacing must be >= 0.14 um
METAL5.SP.1.2	Metal5 to Metal5 spacing must be >= 0.20 um
METAL5.SP.1.3	Metal5 to Metal5 spacing must be >= 0.50 um
METAL5.SP.1.4	Metal5 to Metal5 spacing must be >= 0.90 um
METAL5.SP.1.5	Metal5 to Metal5 spacing must be >= 1.50 um
METAL5.SP.1.6	Metal5 to Metal5 spacing must be >= 2.50 um
METAL5.SP.2	Metal5 to bent Metal5 spacing must be >= 0.18 um
METAL5.W.1	Metal5 width must be >= 0.14 um

METAL5.W.2	Metal5 width must be <= 12.0 um
METAL5.W.3	Bent Metal5 (45 degree angle) width must be >= 0.16
METAL6.A.1	Metal6 area must be >= 0.08 um
METAL6.D.1	Metal6 density must be >= 20% <= 65%
METAL6.D.2	Metal6 density must be <= 60%
METAL6.E.1	Metal6 to Via5 enclosure must be >= 0.005 um
METAL6.E.2	Metal6 to Via5 enclosure on opposite sides must be >= 0.06 um
METAL6.L.1	Metal6 non-90 degree segments must be >= 0.20 um
METAL6.SP.1.1	Metal6 to Metal6 spacing must be >= 0.14 um
METAL6.SP.1.2	Metal6 to Metal6 spacing must be >= 0.20 um
METAL6.SP.1.3	Metal6 to Metal6 spacing must be >= 0.50 um
METAL6.SP.1.4	Metal6 to Metal6 spacing must be >= 0.90 um
METAL6.SP.1.5	Metal6 to Metal6 spacing must be >= 1.50 um
METAL6.SP.1.6	Metal6 to Metal6 spacing must be >= 2.50 um
METAL6.SP.2	Metal6 to bent Metal6 spacing must be >= 0.18 um
METAL6.W.1	Metal6 width must be >= 0.14 um
METAL6.W.2	Metal6 width must be <= 12.0 um
METAL6.W.3	Bent Metal6 (45 degree angle) width must be >= 0.16
METAL7.A.1	Metal7 area must be >= 0.08 um
METAL7.D.1	Metal7 density must be >= 20% <= 65%
METAL7.D.2	Metal7 density must be <= 60%
METAL7.E.1	Metal7 to Via6 enclosure must be >= 0.005 um
METAL7.E.2	Metal7 to Via6 enclosure on opposite sides must be >= 0.06 um
METAL7.L.1	Metal7 non-90 degree segments must be >= 0.20 um
METAL7.SP.1.1	Metal7 to Metal7 spacing must be >= 0.14 um
METAL7.SP.1.2	Metal7 to Metal7 spacing must be >= 0.20 um
METAL7.SP.1.3	Metal7 to Metal7 spacing must be >= 0.50 um
METAL7.SP.1.4	Metal7 to Metal7 spacing must be >= 0.90 um
METAL7.SP.1.5	Metal7 to Metal7 spacing must be >= 1.50 um
METAL7.SP.1.6	Metal7 to Metal7 spacing must be >= 2.50 um
METAL7.SP.2	Metal7 to bent Metal7 spacing must be >= 0.18 um
METAL7.W.1	Metal7 width must be >= 0.14 um
METAL7.W.2	Metal7 width must be <= 12.0 um
METAL7.W.3	Bent Metal7 (45 degree angle) width must be >= 0.16
METAL8.A.1	Metal8 area must be >= 0.2 um
METAL8.D.1	Metal8 density must be >= 20% <= 65%
METAL8.D.2	Metal8 density must be <= 60%
METAL8.E.1	Metal8 to Via7 enclosure must be >= 0.05 um
METAL8.E.2	Metal8 to Via7 enclosure on opposite sides must be >= 0.1 um
METAL8.SP.1.1	Metal8 to Metal8 spacing must be >= 0.40 um
METAL8.SP.1.2	Metal8 to Metal8 spacing must be >= 0.50 um
METAL8.SP.1.3	Metal8 to Metal8 spacing must be >= 0.90 um
METAL8.SP.1.4	Metal8 to Metal8 spacing must be >= 1.50 um
METAL8.SP.1.5	Metal8 to Metal8 spacing must be >= 2.50 um
METAL8.W.1	Metal8 width must be >= 0.44 um
METAL8.W.2	Metal8 width must be <= 12.0 um
METAL9.A.1	Metal9 area must be >= 0.2 um
METAL9.D.1	Metal9 density must be >= 20% <= 65%

METAL9.D.2	Metal9 density must be <= 60%
METAL9.E.1	Metal9 to Via8 enclosure must be >= 0.05 um
METAL9.E.2	Metal9 to Via8 enclosure on opposite sides must be >= 0.1 um
METAL9.SP.1.1	Metal9 to Metal9 spacing must be >= 0.40 um
METAL9.SP.1.2	Metal9 to Metal9 spacing must be >= 0.50 um
METAL9.SP.1.3	Metal9 to Metal9 spacing must be >= 0.90 um
METAL9.SP.1.4	Metal9 to Metal9 spacing must be >= 1.50 um
METAL9.SP.1.5	Metal9 to Metal9 spacing must be >= 2.50 um
METAL9.W.1	Metal9 width must be >= 0.44 um
METAL9.W.2	Metal9 width must be <= 12.0 um
MSLOT1.SP.1	Metal1 Slot to Metal1 Slot spacing must be >= 0.12 um
MSLOT1.W.1_MSLOT1.L.1	Metal1 Slot width/length must be >= 2.0 um
MSLOT2.SP.1	Metal2 Slot to Metal2 Slot spacing must be >= 0.14 um
MSLOT2.W.1_MSLOT2.L.1	Metal2 Slot width/length must be >= 2.0 um
MSLOT3.SP.1	Metal3 Slot to Metal3 Slot spacing must be >= 0.14 um
MSLOT3.W.1_MSLOT3.L.1	Metal3 Slot width/length must be >= 2.0 um
MSLOT4.SP.1	Metal4 Slot to Metal4 Slot spacing must be >= 0.14 um
MSLOT4.W.1_MSLOT4.L.1	Metal4 Slot width/length must be >= 2.0 um
MSLOT5.SP.1	Metal5 Slot to Metal5 Slot spacing must be >= 0.14 um
MSLOT5.W.1_MSLOT5.L.1	Metal5 Slot width/length must be >= 2.0 um
MSLOT6.SP.1	Metal6 Slot to Metal6 Slot spacing must be >= 0.14 um
MSLOT6.W.1_MSLOT6.L.1	Metal6 Slot width/length must be >= 2.0 um
MSLOT7.SP.1	Metal7 Slot to Metal7 Slot spacing must be >= 0.14 um
MSLOT7.W.1_MSLOT7.L.1	Metal7 Slot width/length must be >= 2.0 um
MSLOT8.SP.1	Metal8 Slot to Metal8 Slot spacing must be >= 0.44 um
MSLOT8.W.1_MSLOT8.L.1	Metal8 Slot width/length must be >= 2.0 um
MSLOT9.SP.1	Metal9 Slot to Metal9 Slot spacing must be >= 0.44 um
MSLOT9.W.1_MSLOT9.L.1	Metal9 Slot width/length must be >= 2.0 um
NBL.E.1	Nburied to Nwell enclosure must be >= 0.4 um
NBL.SE.1	Nburied to non-related Nwell spacing must be >= 4.4 um
NBL.SE.2	Nburied to Oxide spacing must be >= 2.2 um
NBL.SE.3	Nwell ring (on Nburied) to P+ Oxide spacing must be >= 0.5 um
NBL.SE.4	Nwell ring (on Nburied) to N+ Oxide spacing must be >= 0.4 um
NBL.SP.1	Nburied to Nburied spacing must be >= 5.0 um
NBL.W.1	Nburied width must be >= 3.2 um
NBL.X.1	Nburied must have an Nwell isolation ring
NHVT.X.1	Nhvt to Oxide enclosure must be == 0.0 on all sides
NHVT.X.2	Nhvt is NOT allowed on Nwell
NHVT.X.3	Nhvt is NOT allowed on P+ Oxide
NHVT.X.4	Nhvt is NOT allowed on Nzvt
NIMP.A.1	Nimp area must be >= 0.15 um
NIMP.E.1	Nimp to Oxide enclosure must be >= 0.14 um
NIMP.E.2	Nimp to Oxide (Nwell tie) enclosure must be >= 0.02 um
NIMP.E.3	Nimp to Poly gate enclosure must be >= 0.18 um
NIMP.E.4	Nimp to gate end enclosure must be >= 0.18 um
NIMP.EA.1	Area in Nimp ring must be >= 0.16 um
NIMP.O.1	Nimp to Oxide overlap must be >= 0.16 um
NIMP.SE.1	Nimp to P+ Oxide spacing must be >= 0.16 um

NIMP.SE.2	Nimp to P+ Oxide spacing must be >= 0.02 um
NIMP.SE.3	Nimp to P+ gate spacing must be >= 0.18 um
NIMP.SP.1	Nimp to Nimp spacing must be >= 0.24 um
NIMP.W.1	Nimp width must be >= 0.24 um
NIMP.X.1	Nimp is NOT allowed over Pimp
NW.E.1	Nwell to N+ Oxide enclosure must be >= 0.12 um
NW.E.2	Nwell to P+ Oxide enclosure must be >= 0.12 um
NW.E.3	Nwell to N+ 2.5V Oxide enclosure must be >= 0.7 um
NW.E.4	Nwell to P+ 2.5V Oxide enclosure must be >= 0.7 um
NW.SE.1	Nwell to Oxide spacing must be >= 0.3 um
NW.SE.2	Nwell to P+ Oxide spacing must be >= 0.3 um
NW.SE.3	Nwell to N+ 2.5V Oxide spacing must be >= 0.5 um
NW.SE.4	Nwell to P+ 2.5V Oxide spacing must be >= 0.5 um
NW.SP.1	Nwell to Nwell spacing (same potential) must be >= 0.6 um
NW.SP.2	Nwell to Nwell spacing (diferent potential) must be >= 1.2 um
NW.SP.2	Nwell to Nwell spacing (diferent potential) must be >= 1.2 um
NW.SP.2	Nwell to Nwell spacing (diferent potential) must be >= 1.2 um
NW.W.1	Nwell width must be >= 0.6 um
NWR.E.1	Oxide to Nwell (in resistor) enclosure must be >= 1.2 um
NWR.E.2	Nwell (in resistor) to Cont enclosure must be >= 0.32 um
NWR.O.1	SiProt to Nimp overlap must be >= 0.45 um
NWR.SE.1	Nwell (in resistor) to SiProt spacing must be >= 0.32 um
NWR.X.1	Thick Oxide is NOT allowed over Nwell resistor
NZVT.E.1	Poly to Oxide enclosure must be >= 0.2 um
NZVT.E.1.DFM	Poly to Oxide enclosure must be >= 0.22 um for DFM
NZVT.L.1	Native Device Poly gate length must be >= 0.9 um
NZVT.O.1	Nzvt to Oxide enclosure must be == 0.3
NZVT.SE.1	Nzvt to Oxide spacing must be >= 0.28 um
NZVT.SE.2	Nzvt to Nwell spacing must be >= 1.2 um
NZVT.SP.1	Nzvt to Nzvt spacing must be >= 0.6 um
NZVT.W.1	Nzvt width must be >= 0.7 um
NZVT.W.2	Native Device Poly gate width must be >= 0.65 um
NZVT.X.3	P+ Oxide is NOT allowed in Nzvt
NZVT.X.4	Only one Oxide region may be in an Nzvt region
OXIDE.A.1	Oxide area must be >= 0.06 um
OXIDE.EA.1	Oxide enclosed area must be >= 0.10 um
OXIDE.L.1_OXIDE.L.2	Maximum Oxide length between two contacts (when the Oxide width is <= 0.18 um) must be <= 22.0um and Maximum Oxide length between one contact and the end of the Oxide line (when the Oxide width is <= 0.18um) must be <= 11.0 um
OXIDE.SE.1	Oxide to Oxide_thk spacing must be >= 0.28 um
OXIDE.SP.1	N+ Oxide to N+ Oxide spacing must be >= 0.15 um
OXIDE.SP.2	P+ Oxide to P+ Oxide spacing must be >= 0.15 um
OXIDE.SP.3	P+ Oxide to P+ Oxide spacing must be >= 0.15 um
OXIDE.SP.4	Oxide bent 45 degree to Oxide spacing must be >= 0.18 um
OXIDE.W.1	Oxide width must be >= 0.1 um
OXIDE.W.2.1.1	1.2V N-channel gate width must be >= 0.12 um
OXIDE.W.2.1.2	2.5V N-channel gate width must be >= 0.15 um

OXIDE.W.2.2.1	1.2V P-channel gate width must be >= 0.12 um
OXIDE.W.2.2.2	2.5V P-channel gate width must be >= 0.15 um
OXIDE.W.3	Oxide (45 degree) width must be >= 0.13 um
OXIDE.X.1	Oxide must be covered by Nimp or Pimp or Nzvt
OXIDER.E.1	SiProt to Oxide resistor enclosure must be >= 0.25 um
OXIDER.L.1	Oxide resistor length must be >= 8.0 um
OXIDER.SE.1	SiProt to Oxide resistor Cont spacing must be >= 0.25 um
OXIDER.SE.2	Oxide resistor to Nimp spacing must be >= 0.3 um
OXIDER.SE.2	Oxide resistor to Pimp spacing must be >= 0.3 um
OXIDER.W.1.1	Oxide resistor width must be >= 0.2 um
OXIDER.W.1.2	Oxide resistor width must be >= 1.5 um
OXIDER.X.1	Oxide resistors must have N+ or P+ Implant
OXIDETHK.E.1	Oxide_thk to Oxide enclosure must be >= 0.30 um
OXIDETHK.E.2	Oxide_thk to Poly gate enclosure must be >= 0.36 um
OXIDETHK.SE.1	2.5V N+ Oxide to 2.5V N+ Oxide spacing must be >= 0.20 um
OXIDETHK.SE.2	2.5V P+ Oxide to 2.5V P+ Oxide spacing must be >= 0.20 um
OXIDETHK.SE.3	2.5V N+ Oxide to 2.5V P+ Oxide spacing must be >= 0.25 um
OXIDETHK.SE.5	Oxide_thk to Poly gate spacing must be >= 0.34 um
OXIDETHK.SP.1	Oxide_thk to Oxide_thk spacing must be >= 0.35 um
OXIDETHK.SP.2	Oxide_thk (bent 45 degree) to Oxide_thk spacing must be >= 0.75 um
OXIDETHK.W.1	Oxide_thk width must be >= 0.7 um
PHVT.X.1	Phvt to Oxide enclosure must be == 0.0 on all sides
PHVT.X.2	Phvt is NOT allowed outside Nwell
PHVT.X.3	Phvt is NOT allowed on N+ Oxide
PHVT.X.4	Phvt is NOT allowed on Nzvt
PIMP.A.1	Pimp area must be >= 0.15 um
PIMP.E.1	Pimp to Oxide enclosure must be >= 0.14 um
PIMP.E.2	Pimp to Oxide (substrate tie) enclosure must be >= 0.02 um
PIMP.E.3	Pimp to Poly gate enclosure must be >= 0.18 um
PIMP.E.4	Pimp to gate end enclosure must be >= 0.18 um
PIMP.EA.1	Area in Pimp ring must be >= 0.16 um
PIMP.O.1	Pimp to Oxide overlap must be >= 0.16 um
PIMP.SE.1	Pimp to N+ Oxide spacing must be >= 0.16 um
PIMP.SE.2	Pimp to N+ Oxide spacing must be >= 0.02 um
PIMP.SE.3	Pimp to N+ gate spacing must be >= 0.18 um
PIMP.SP.1	Pimp to Pimp spacing must be >= 0.24 um
PIMP.W.1	Pimp width must be >= 0.24 um
POLY.A.1	Poly area must be >= 0.1 um
POLY.D.1	Poly density must be <= 50%
POLY.E.1	Poly to N+ Oxide enclosure must be >= 0.18 um
POLY.E.1.DFM	Poly to N+ Oxide enclosure must be >= 0.20 um for DFM
POLY.E.2	Poly to P+ Oxide enclosure must be >= 0.18 um
POLY.E.2.DFM	Poly to P+ Oxide enclosure must be >= 0.20 um for DFM
POLY.E.3	Oxide to Poly enclosure must be >= 0.2 um
POLY.SE.1_POLY.SE.2	Poly to Oxide spacing must be >= 0.1 um
POLY.SE.3	Poly width, between two contacts spaced > 25.0um, must be >= 0.14um
POLY.SP.1	Poly resistor to Poly resistor spacing must be >= 0.6 um
POLY.SP.2	Poly gate to Poly gate spacing must be >= 0.12 um

POLY.SP.2.DFM	Poly gate to Poly gate spacing must be >= 0.14 um
POLY.SP.3	Poly interconnect to Poly interconnect spacing must be >= 0.12 um
POLY.SP.4	Bent Poly to bent Poly spacing must be >= 0.22 um
POLY.W.1	1.2V N+ Poly gate length must be >= 0.1 um
POLY.W.2	1.2V P+ Poly gate length must be >= 0.1 um
POLY.W.3	2.5V N+ Poly gate length must be >= 0.28 um
POLY.W.4	2.5V P+ Poly gate length must be >= 0.28 um
POLY.W.5	Poly interconnect width must be >= 0.1 um
POLY.W.6	Bent Poly width must be >= 0.18 um
POLY.X.1	Poly gate cannot have bends
POLY.X.2	Poly resistor cannot have bends
POLYR.E.1	SiProt to Poly resistor enclosure must be >= 0.28 um
POLYR.E.2	Nimp to Poly used in resistor enclosure must be >= 0.15 um
POLYR.E.3	Pimp to Poly used in resistor enclosure must be >= 0.15 um
POLYR.L.1	Poly resistor length must be >= 8.0 um
POLYR.SE.1	SiProt to Poly resistor Cont spacing must be >= 0.25 um
POLYR.SE.2	Poly resistor to Nimp spacing must be >= 0.3 um
POLYR.SE.2	Poly resistor to Nzvt spacing must be >= 0.3 um
POLYR.SE.2	Poly resistor to Pimp spacing must be >= 0.3 um
POLYR.W.1.1	Poly resistor width must be >= 0.2 um
POLYR.W.1.2	Poly width must be >= 1.5 um
POLYR.X.1	Poly resistors must have N+ or P+ Implant
SIPROT.A.1	SiProt area must be >= 1.2 um
SIPROT.E.1	SiProt to Oxide enclosure must be >= 0.25 um
SIPROT.E.2	Oxide to SiProt enclosure must be >= 0.24 um
SIPROT.E.3	SiProt to Poly enclosure must be >= 0.28 um
SIPROT.EA.1	Area in SiProt ring must be >= 1.2 um
SIPROT.SE.1	SiProt to Cont spacing must be >= 0.24 um
SIPROT.SE.2	SiProt to Oxide spacing must be >= 0.24 um
SIPROT.SE.3	SiProt to Poly gate spacing must be >= 0.44 um
SIPROT.SE.4	SiProt to Poly (on field) spacing must be >= 0.35 um
SIPROT.SP.1	SiProt to SiProt spacing must be >= 0.44 um
SIPROT.W.1	SiProt width must be >= 0.44 um
VIA1.E.1	Metal1 to Via1 enclosure must be >= 0.005 um
VIA1.E.2	Metal1 to Via1 enclosure on opposite sides must be >= 0.06 um
VIA1.SP.1	Via1 to Via1 spacing must be >= 0.15 um
VIA1.SP.2	Via1 to Via1 spacing must be >= 0.20 um
VIA1.W.1	Via1 shapes must be 0.14x0.14 rectangles
VIA1.X.1	Metal1 must connect to Metal2 with >= 2 Via1 spaced < 0.30 um or >= 4 Via1 spaced < 0.60 um
VIA1.X.2	Metal1 must connect to Metal2 with >= 4 Via1 spaced < 0.30 um or >= 9 Via1 spaced < 0.60 um
VIA2.E.1	Metal2 to Via2 enclosure must be >= 0.005 um
VIA2.E.2	Metal2 to Via2 enclosure on opposite sides must be >= 0.06 um
VIA2.SP.1	Via2 to Via2 spacing must be >= 0.15 um
VIA2.SP.2	Via2 to Via2 spacing must be >= 0.20 um
VIA2.W.1	Via2 shapes must be 0.14x0.14 rectangles

VIA2.X.1	Metal2 must connect to Metal3 with >= 2 Via2 spaced < 0.30 um or >= 4 Via2 spaced < 0.60 um
VIA2.X.2	Metal2 must connect to Metal3 with >= 4 Via2 spaced < 0.30 um or >= 9 Via2 spaced < 0.60 um
VIA3.E.1	Metal3 to Via3 enclosure must be >= 0.005 um
VIA3.E.2	Metal3 to Via3 enclosure on opposite sides must be >= 0.06 um
VIA3.SP.1	Via3 to Via3 spacing must be >= 0.15 um
VIA3.SP.2	Via3 to Via3 spacing must be >= 0.20 um
VIA3.W.1	Via3 shapes must be 0.14x0.14 rectangles
VIA3.X.1	Metal3 must connect to Metal4 with >= 2 Via3 spaced < 0.30 um or >= 4 Via3 spaced < 0.60 um
VIA3.X.2	Metal3 must connect to Metal4 with >= 4 Via3 spaced < 0.30 um or >= 9 Via3 spaced < 0.60 um
VIA4.E.1	Metal4 to Via4 enclosure must be >= 0.005 um
VIA4.E.2	Metal4 to Via4 enclosure on opposite sides must be >= 0.06 um
VIA4.SP.1	Via4 to Via4 spacing must be >= 0.15 um
VIA4.SP.2	Via4 to Via4 spacing must be >= 0.20 um
VIA4.W.1	Via4 shapes must be 0.14x0.14 rectangles
VIA4.X.1	Metal4 must connect to Metal5 with >= 2 Via4 spaced < 0.30 um or >= 4 Via4 spaced < 0.60 um
VIA4.X.2	Metal4 must connect to Metal5 with >= 4 Via4 spaced < 0.30 um or >= 9 Via4 spaced < 0.60 um
VIA5.E.1	Metal5 to Via5 enclosure must be >= 0.005 um
VIA5.E.2	Metal5 to Via5 enclosure on opposite sides must be >= 0.06 um
VIA5.SP.1	Via5 to Via5 spacing must be >= 0.15 um
VIA5.SP.2	Via5 to Via5 spacing must be >= 0.20 um
VIA5.W.1	Via5 shapes must be 0.14x0.14 rectangles
VIA5.X.1	Metal5 must connect to Metal6 with >= 2 Via5 spaced < 0.30 um or >= 4 Via5 spaced < 0.60 um
VIA5.X.2	Metal5 must connect to Metal6 with >= 4 Via5 spaced < 0.30 um or >= 9 Via5 spaced < 0.60 um
VIA6.E.1	Metal6 to Via6 enclosure must be >= 0.005 um
VIA6.E.2	Metal6 to Via6 enclosure on opposite sides must be >= 0.06 um
VIA6.SP.1	Via6 to Via6 spacing must be >= 0.15 um
VIA6.SP.2	Via6 to Via6 spacing must be >= 0.20 um
VIA6.W.1	Via6 shapes must be 0.14x0.14 rectangles
VIA6.X.1	Metal6 must connect to Metal7 with >= 2 Via6 spaced < 0.30 um or >= 4 Via6 spaced < 0.60 um
VIA6.X.2	Metal6 must connect to Metal7 with >= 4 Via6 spaced < 0.30 um or >= 9 Via6 spaced < 0.60 um
VIA7.E.1	Metal7 to Via7 enclosure must be >= 0.03 um
VIA7.E.2	Metal7 to Via7 enclosure on opposite sides must be >= 0.08 um
VIA7.SP.1	Via7 to Via7 spacing must be >= 0.36 um
VIA7.W.1	Via7 shapes must be 0.36x0.36 rectangles
VIA8.E.1	Metal8 to Via8 enclosure must be >= 0.03 um
VIA8.E.2	Metal8 to Via8 enclosure on opposite sides must be >= 0.08 um
VIA8.SP.1	Via8 to Via8 spacing must be >= 0.36 um
VIA8.W.1	Via8 shapes must be 0.36x0.36 rectangles
VIAk.X.3_VIAk.X.4	Metal1 through Metal6 stack must have two or more stacked Vias at all levels

VIAk.X.3_VIAk.X.4	Metal2 through Metal7 stack must have two or more stacked Vias at all levels